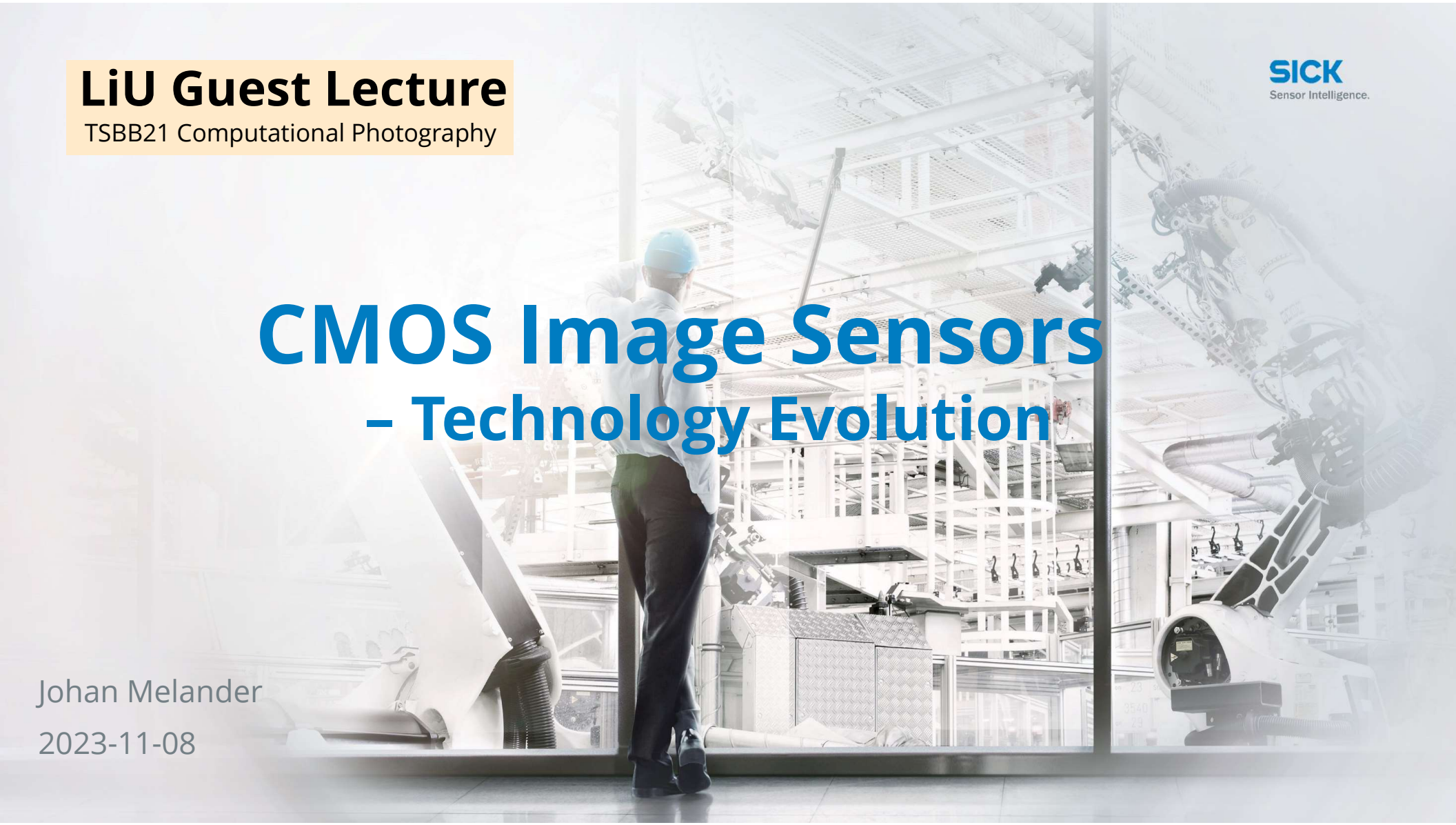
LiU Guest Lecture

TSBB21 Computational Photography

SICK
Sensor Intelligence.



CMOS Image Sensors
– Technology Evolution

Johan Melander

2023-11-08

Who am I?

- Johan Melander
  - 1995: MSc. Computer Science and Electrical Engineering, LiU
  - 1997: Lic. Eng. from Department of Electrical Engineering, LiU

  - 1997 I started at the LiU spin-off *Integrated Vison Products AB* (IVP AB) designing CMOS image sensors
    - IVP AB was founded 1985 by Robert Forchheimer and Anders Ödmark. IVP's core technology was their custom made CMOS image sensors.

  - 2003 IVP AB was fully integrated into the German industrial sensor company SICK AG (~12.000 employees, >2B EUR sales), where we now represent SICK's *Innovation Center for Machine Vision*.
  - At *SICK IVP AB*, the technical work I have done has mainly focused on image sensors.

Agenda

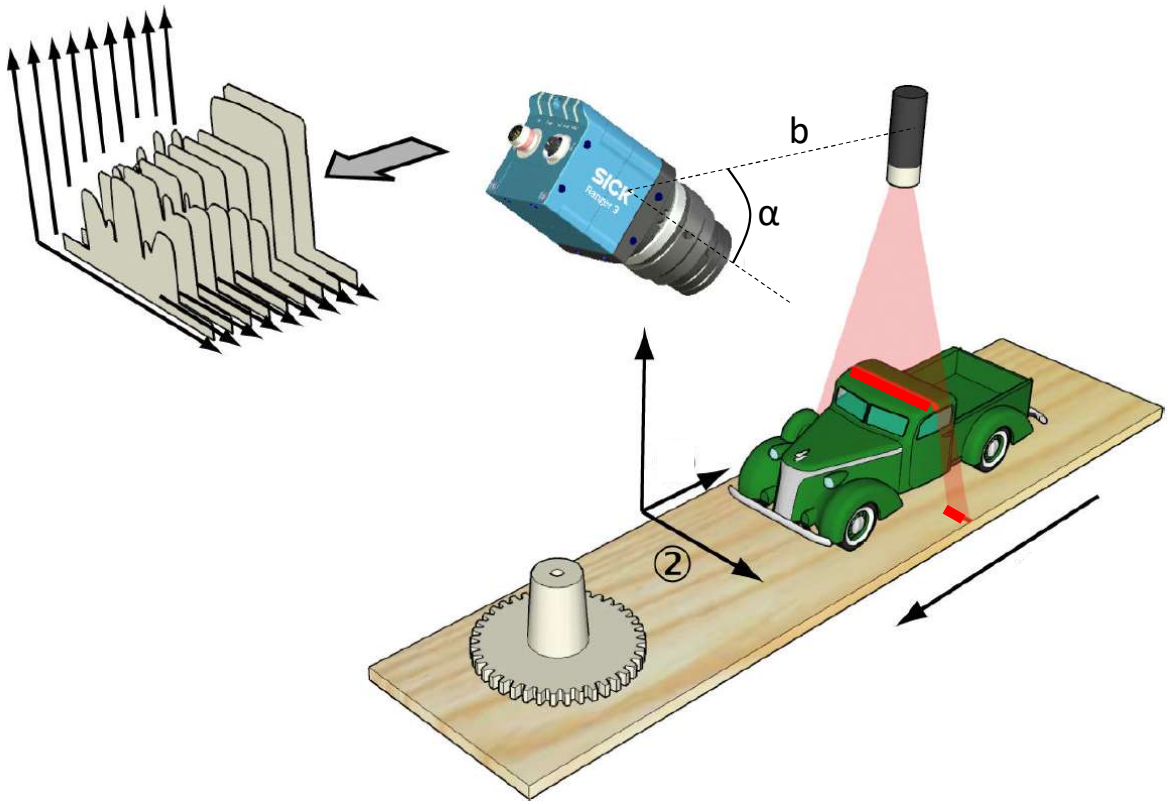
… the advances in CMOS Image Sensor (CIS) semiconductor technology…

… that for instance has enabled SICK to build one of the world's fastest laser triangulation sensors.

Why do we work with CMOS image sensors at SICK?

Why do we work with CMOS image sensors at SICK?

At SICK (among other tings) we develop 3D cameras for industrial automation applications.
For the SICK *Ranger*/*Ruler* products we use the **laser triangulation** principle to acquire **3D data**.



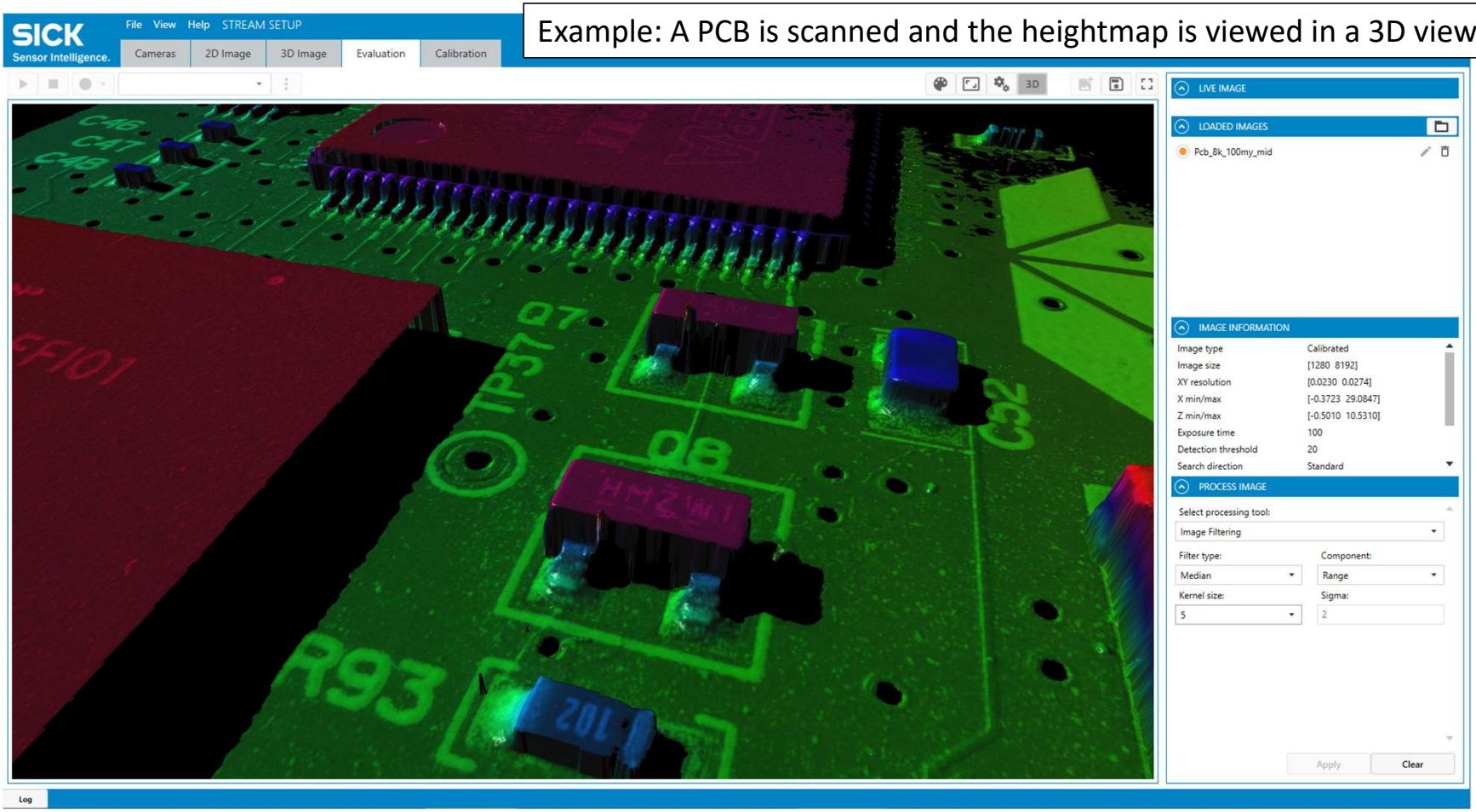
Laser Triangulation Principle

- A target is moving through a projected laser line.
- For each trigger a new image with laser line is acquired by the camera…
- … and given the "geometry" of the setup the *height* (3D data) can now be calculated
- The *height profiles* are put together to form the complete 3D data (*height map*) of the object

CMOS Image Sensors – Technology Evolution

Why do we work with CMOS image sensors at SICK?

Example: A PCB is scanned and the heightmap is viewed in a 3D viewer



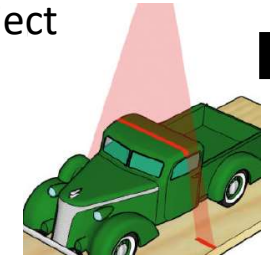
SICK
Sensor Intelligence.

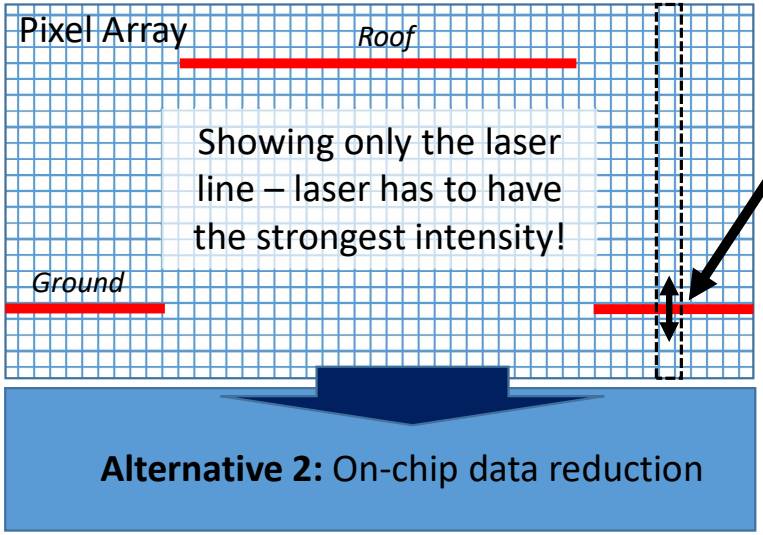
CMOS Image Sensors – Technology Evolution

Why do we work with CMOS image sensors at SICK?

And that is why I work with custom CMOS image sensors at SICK

The image sensor in the laser triangulation camera "sees" the laser profile projected on the object





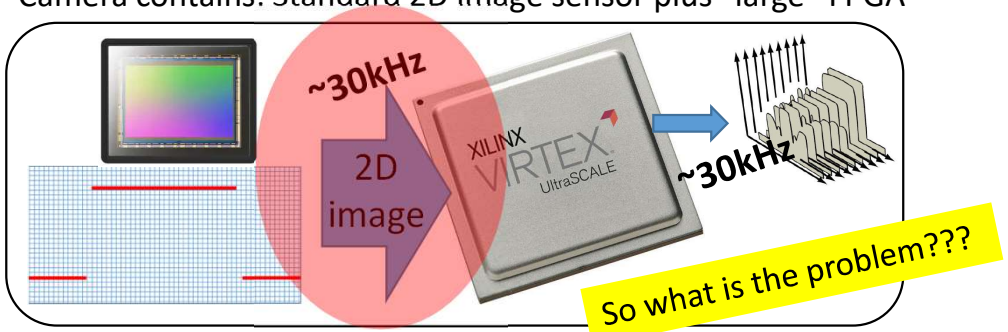
The position of the laser line in a column of the image sensor is proportional to the height of the object (3D information)

Position of laser in each column

This enables us to do the fastest and most compact laser triangulation systems in the world

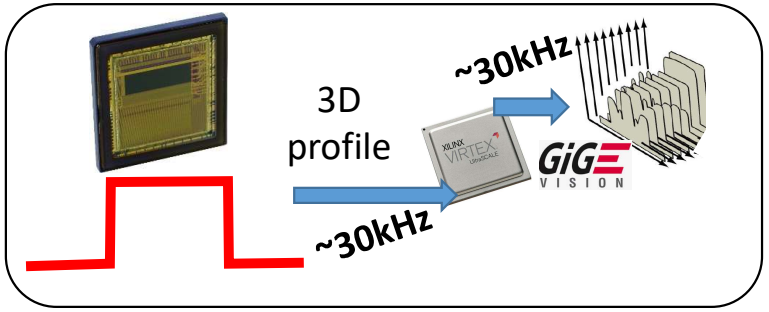
Alternative 1 – "Brute force"

Camera contains: Standard 2D image sensor plus "large" FPGA



Alternative 2 – "SICK approach"

Camera contains: Custom CMOS image sensor plus "medium" FPGA



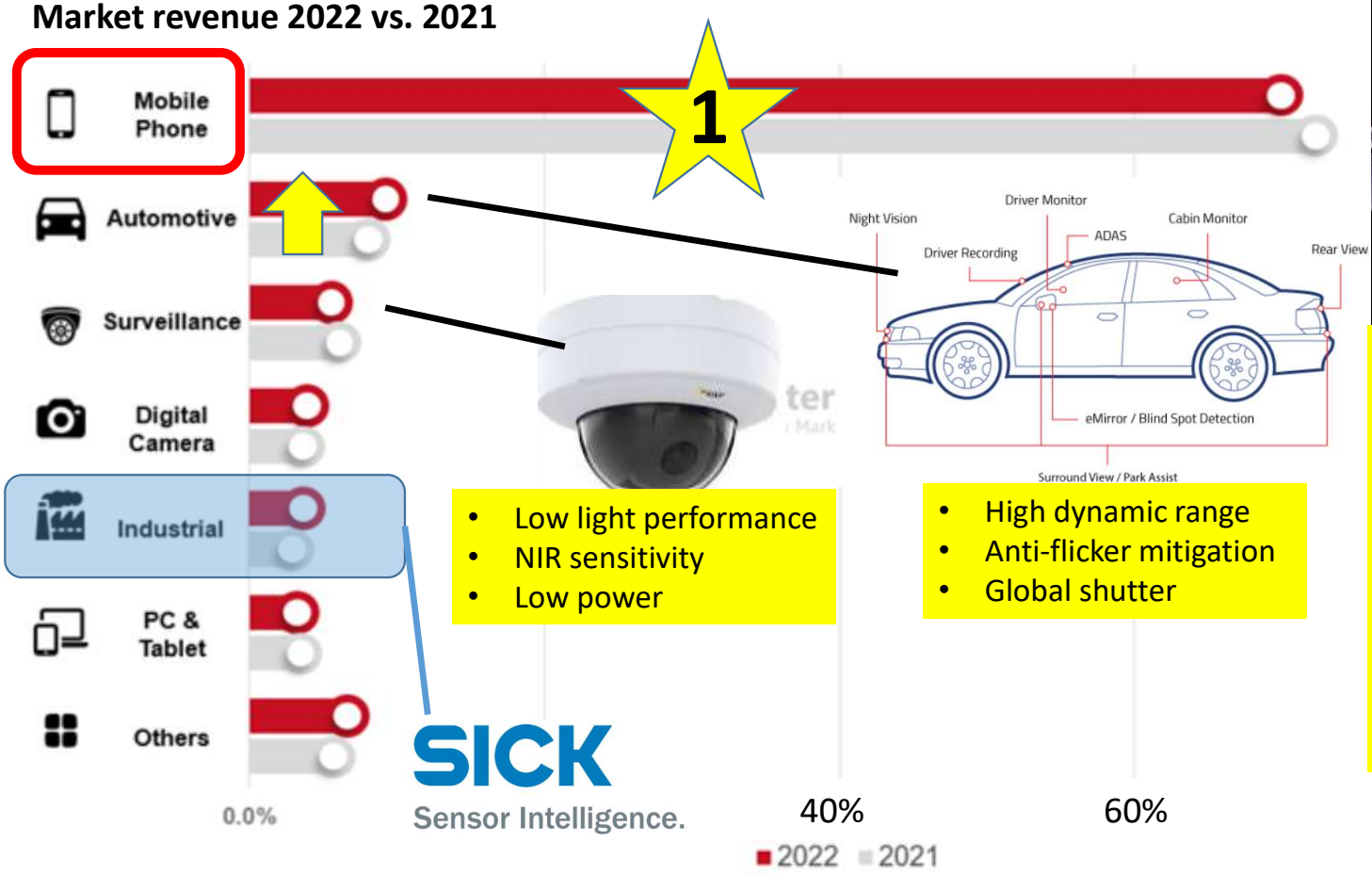
SICK
Sensor Intelligence.

What is driving the technology evolution of CMOS image sensors?

CMOS Image Sensors – Technology Evolution

What is driving the technology evolution

CMOS Image Sensor (CIS) where are they used?
Market revenue 2022 vs. 2021



- Low light performance
- NIR sensitivity
- Low power

- High dynamic range
- Anti-flicker mitigation
- Global shutter

The “Megapixel race” for Smartphones means higher resolution imagers in the same space/volume => and this leads to smaller and smaller pixels.

So what has propelled the CIS technology inventions for many years is the need for high quality small pixels.

Samsung: 200Mpix, 0.64µm pixel size
2023: 0.56µm pixel size (Samsung/Omnivision)

Source: https://www.counterpointresearch.com/global-cis-market-annual-revenue-falls-for-first-time-in-a-decade/

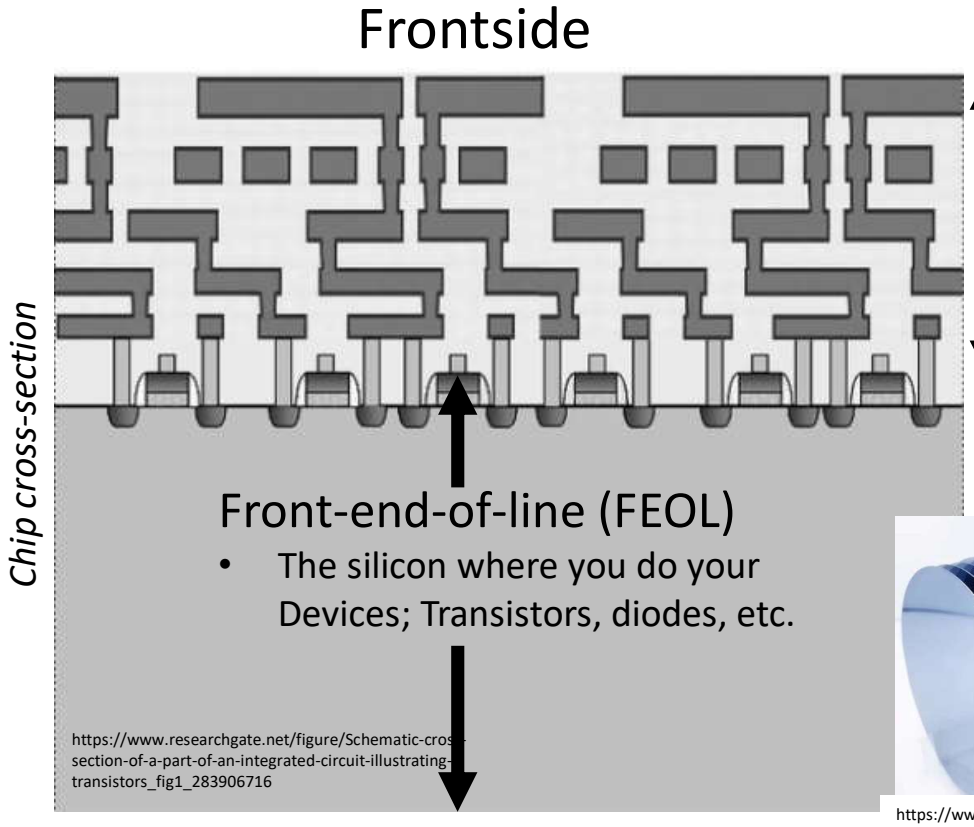
For CMOS imagers we today (since the mid 90:s) need a specialized semiconductor process – why?

CMOS Image Sensors – Technology Evolution

Why a specialized CMOS manufacturing process?

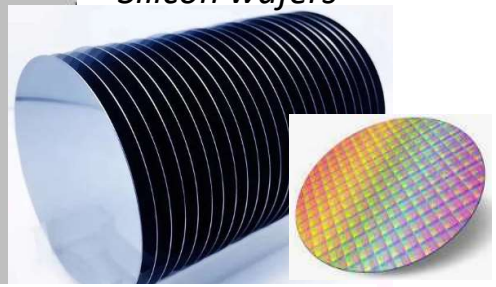
A **standard CMOS process** is used to manufacture e.g. an Intel CPU, or the Qualcomm Snapdragon, or an Nvidia GPU.

- Process is optimized for *logic*
- Scaling to smaller geometries and higher performance still follows "*Moore's law*"
- Today, state of the art *process nodes* are at 3nm-5nm
  (2023, commercial uC: Apples M2 Ultra, 134B trans, TSMC 5nm)



https://www.researchgate.net/figure/Schematic-cross-section-of-a-part-of-an-integrated-circuit-illustrating-transistors_fig1_283906716

Silicon wafers



https://www.msesupplies.com/products/mse-pro-1-cassette-qty-25-of-100-mm-p-type-b-doped-prime-grade-silicon-wafer-100-ssp-10-20-ohm-cm?variant=23715278815290

SICK
Sensor Intelligence.

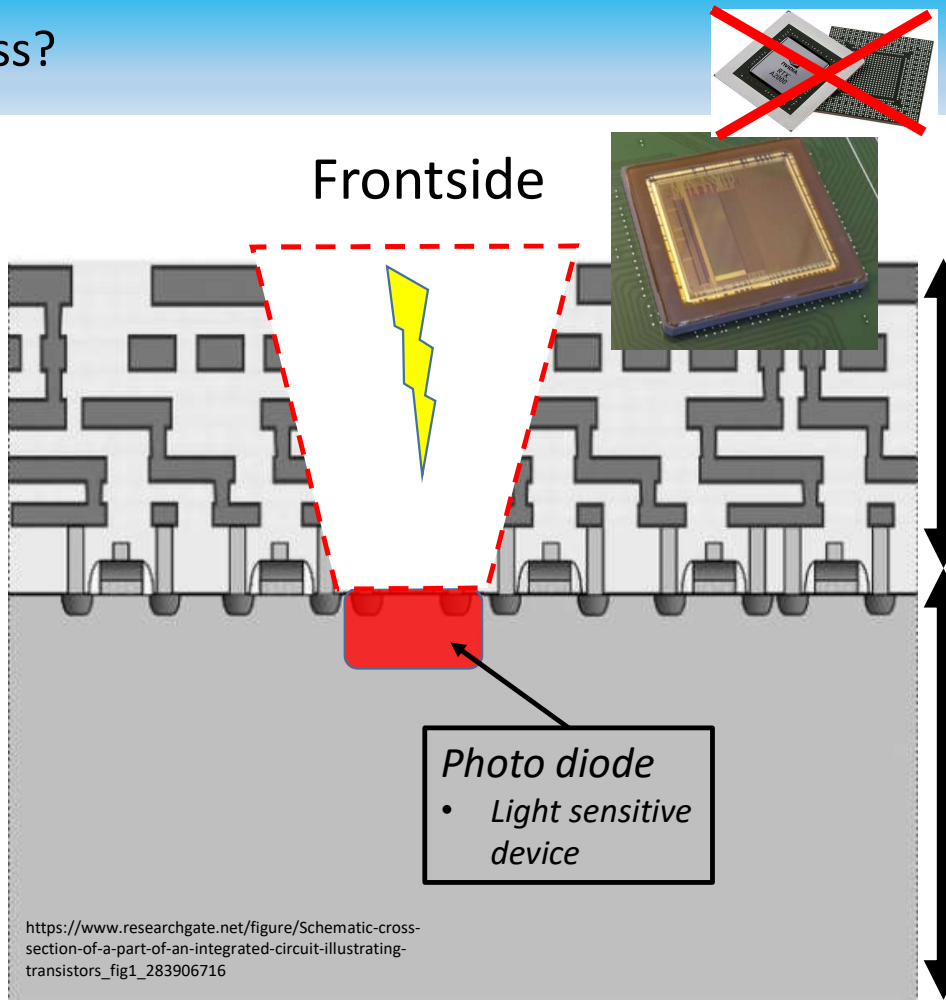
Why a specialized CMOS manufacturing process?

A CMOS Image Sensor (*CIS*) process is very similar to a CMOS process, but …

… today contains **highly specialized process steps** in order to make good optical detection possible (since mid 90's).

First obvious things (not needing a specialize process)are that you need a good photo sensitive device (photo diode) …
… and that you cannot route any wires on top of the pixel
… and need a glass lid on top of the package!

So, besides that, what are the most important specialized process steps in a modern CIS process?
- That is the focus of the rest of this talk

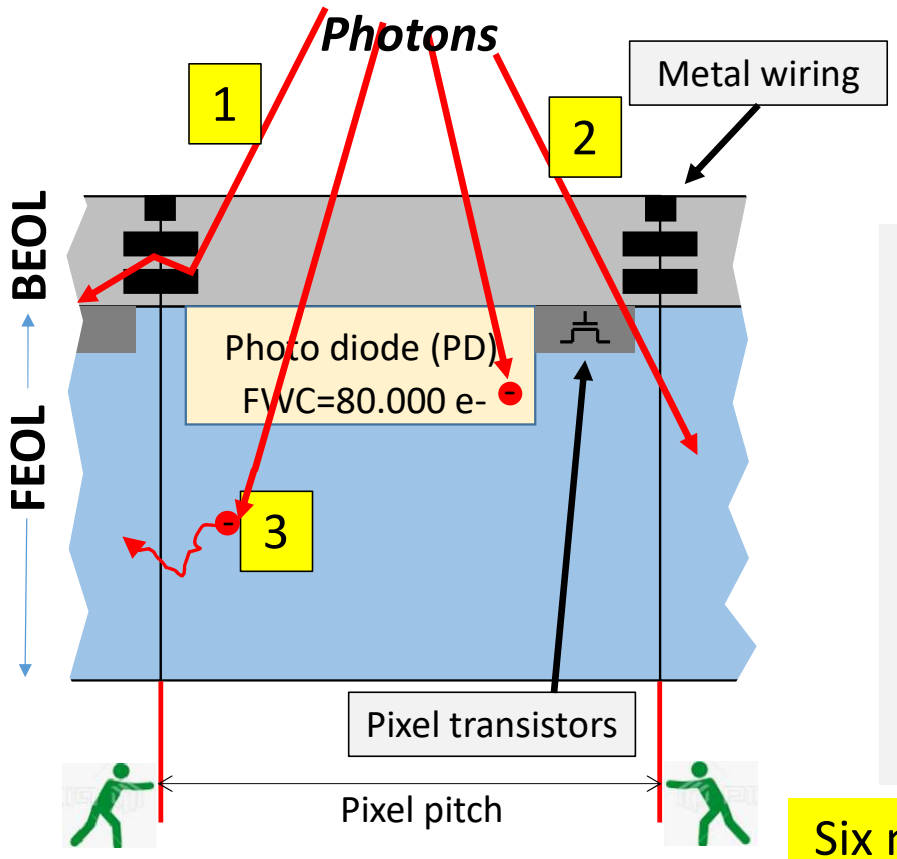


CIS technology enablers

…the 6 most important

CIS Technology Enablers – Cross-talk and Full Well Capacity (FWC)

First, two key terms: *Cross-talk* and *Full Well Capacity* (FWC)



1. Optical cross-talk in the BEOL
2. Optical cross-talk in the FEOL
3. Electrical cross-talk in the FEOL

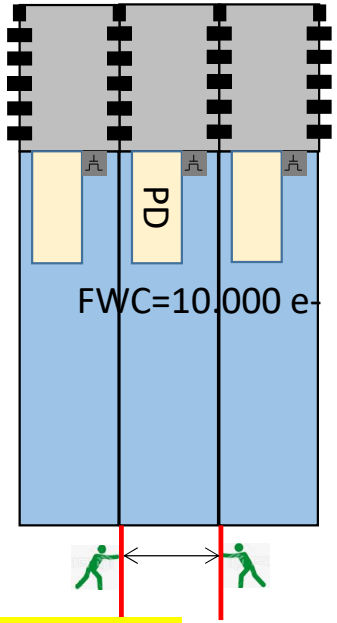
If you just take the next technology node and shrink the pixel;

- Photo diode Full Well Capacity (FWC) decreases => *poorer image quality*
- Cross-talk has a higher relative impact => *poorer image quality*

… so the enablers for a CIS process supporting **high-quality small pixels** boils down to;

1. Maintain a good enough FWC and …
2. … reduce the cross-talk

Small pixels in a modern technology



Six most important process steps will now follow!

SICK
Sensor Intelligence.

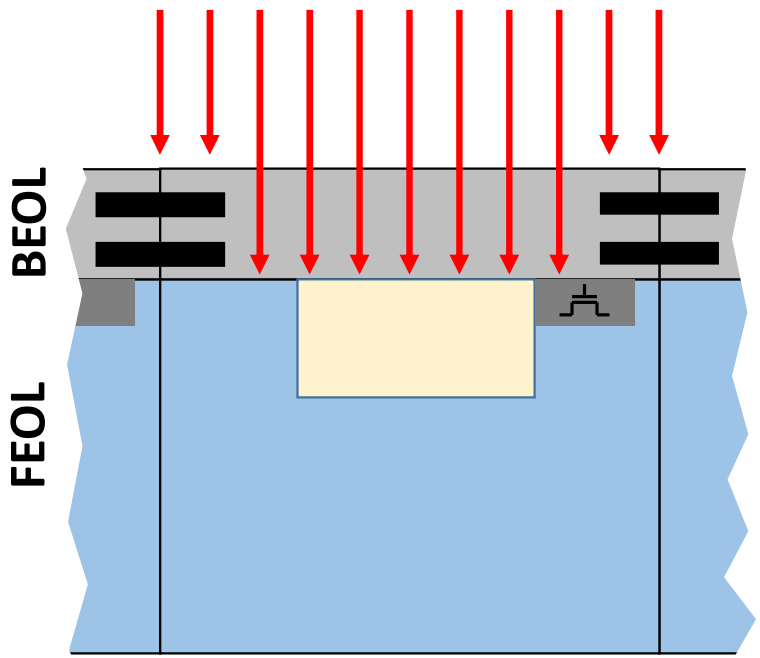
CIS Technology Enablers – Micro Lenses

1

Micro lenses (already in the early 90's)

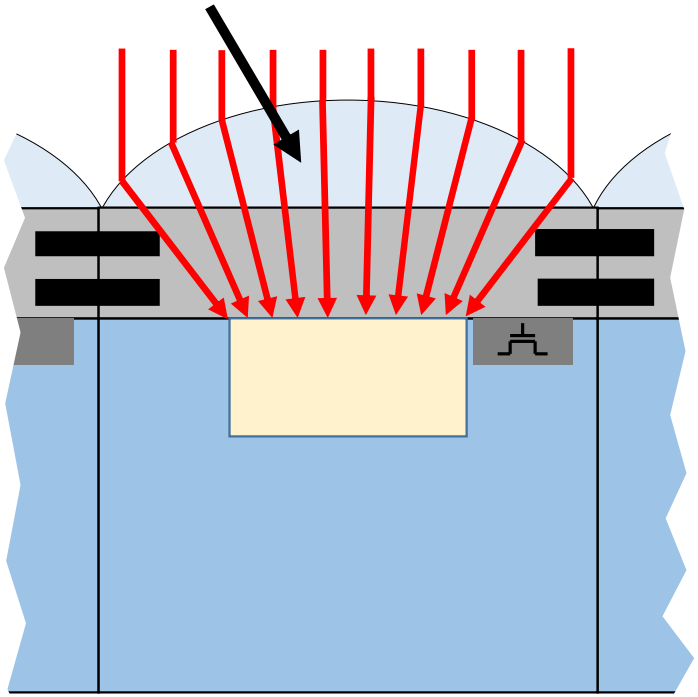
- Focus the light (photons) to find its way to the photo diode

Pixel sizes >10um
- Reduced cross-talk
- "Less light is wasted"



Put *micro lenses* on top of the pixel to direct a "larger portion" of the incoming photons to the photodiode.

Micro lense. Applied after BEOL in a special post-processing step.

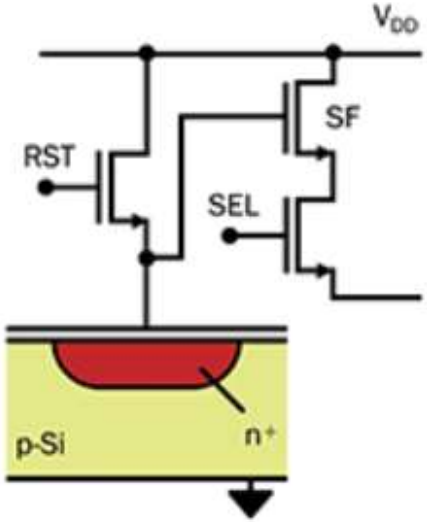


CIS Technology Enablers – The Pinned Photo Diode, PPD

2a **The Pinned Photo Diode, PPD (first seen in products 1995)**

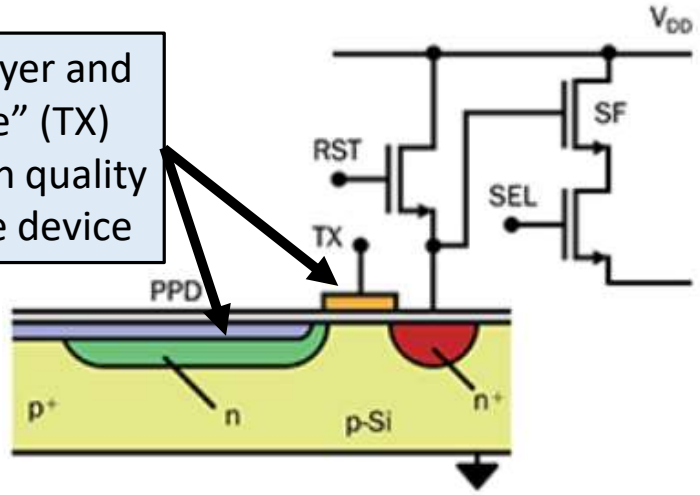
- Pixel structure inherited from the CCD image sensors
- Requires carefully engineered process steps in the FEOL

Active Pixel with a Photo Diode (PD, 3T)



Active Pixel with Pinned Photo Diode (PPD, 4T)

Extra doping layer and a “transfer gate” (TX) results in a high quality photo sensitive device



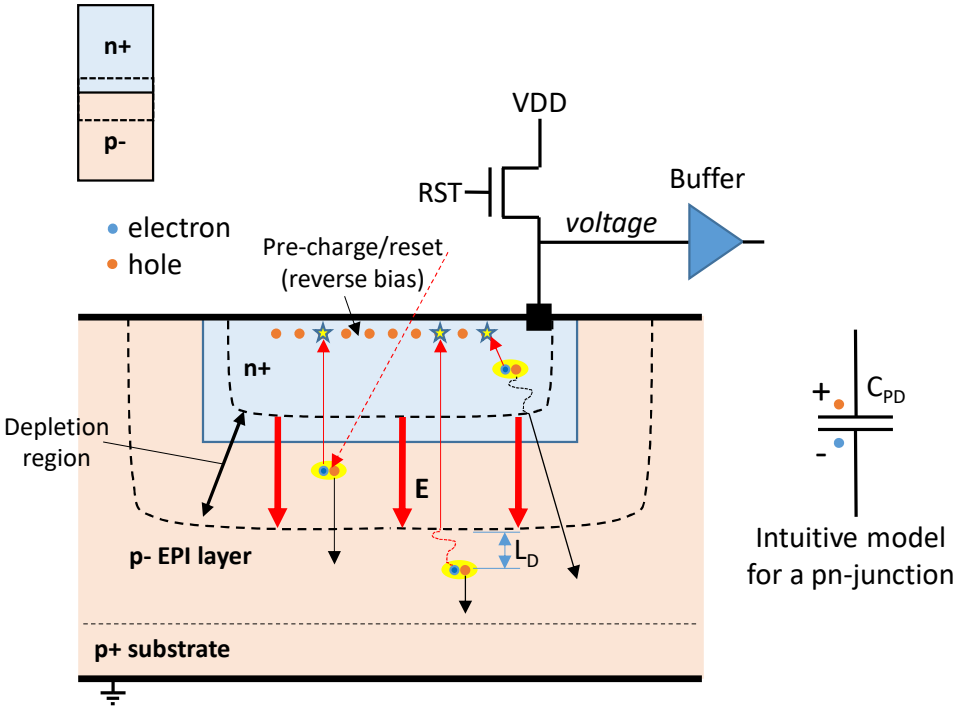
Images from:
https://www.photonics.com/Articles/Advances_in_CMOS_Image_Sensors_Open_Doors_to_Many/a57683

SICK
Sensor Intelligence.

CIS Technology Enablers – The Pinned Photo Diode, PPD

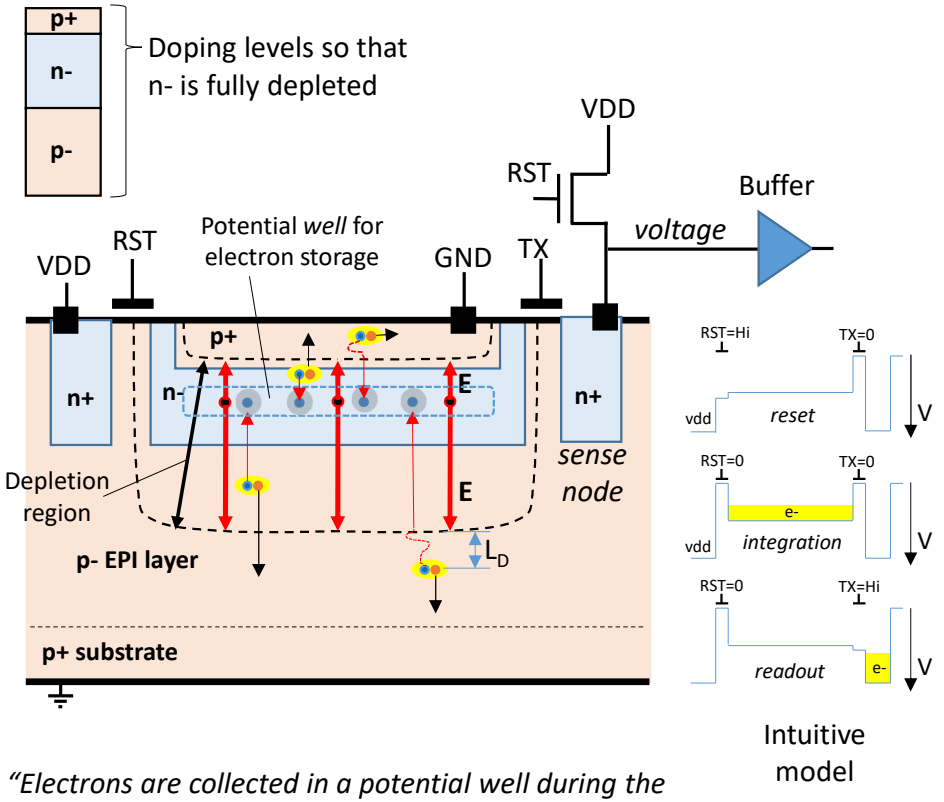
2b

3T Photo Diode Active Pixel



"Collected electrons will discharge the pre-charged photo diode capacitance during the integration time. The remaining voltage over the pn-junction represents the illumination over the exposure time"

4T Pinned Photo Diode Active Pixel



"Electrons are collected in a potential well during the integration time. At end of exposure the electrons are transferred to the sense node where the voltage represents the illumination over exposure time "

SICK
Sensor Intelligence.

CIS Technology Enablers – The Pinned Photo Diode, PPD

2c

Advantages of the Pinned Photo Diode (PPD)

Pixel sizes ~10um
- In general a lower noise pixel => maintained image quality with lower FWC

- Charge collection (potential well) and sense node separated
  - You can optimize them independently (not possible in a photodiode)

- Charge collection (potential well) separated from the surface
  - Avoiding *surface-states* and *surface defects*, resulting in lower dark current and lower noise

- Complete charge transfer is possible from potential well to sense node
  - Correlated Double Sampling (CDS) in readout can be effectively implemented in pixel
  - Low image lag

- Better charge collection close to the surface
  - Higher Quantum Efficiency (QE) for short wave lengths (blue)

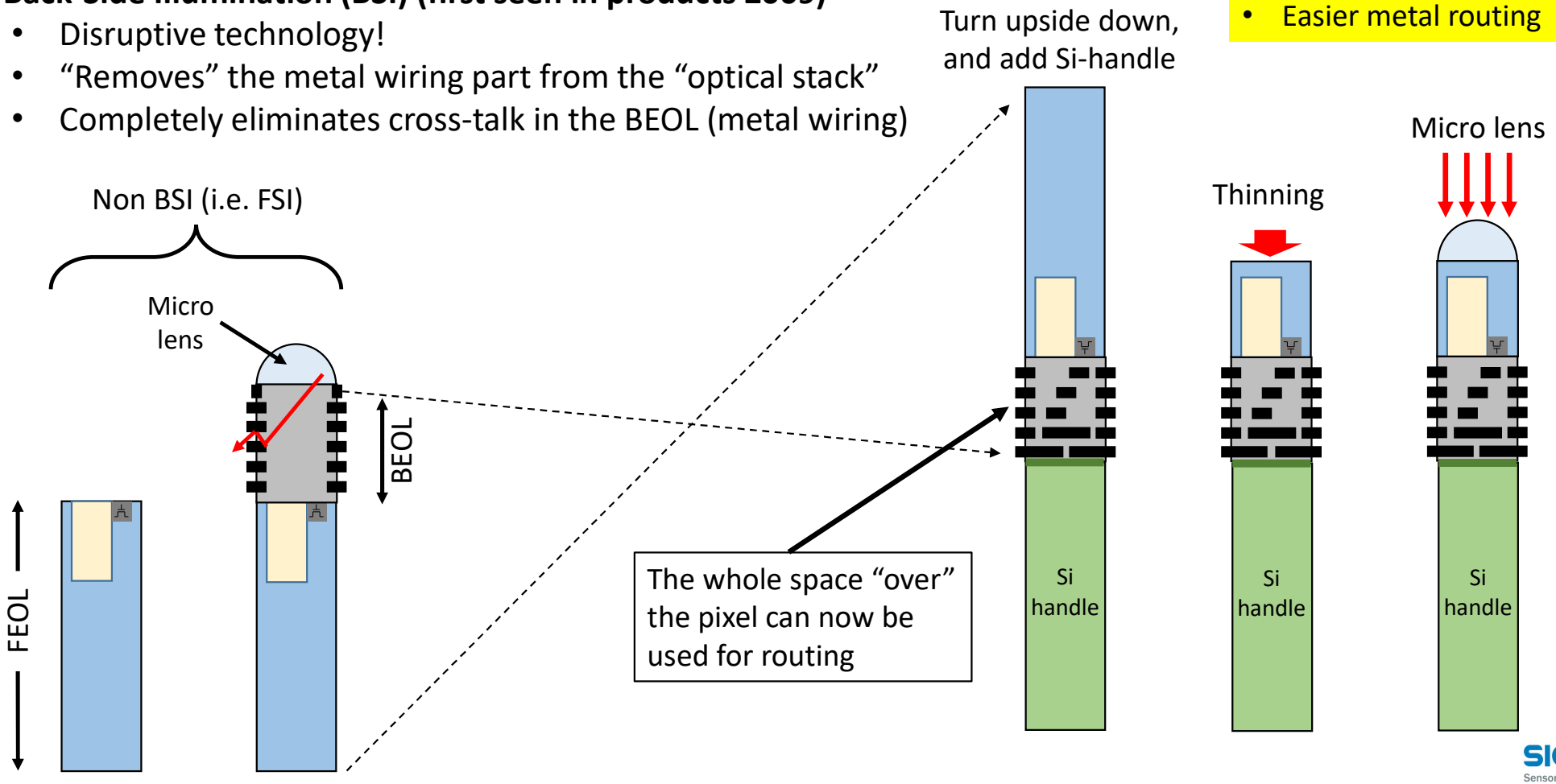
CIS Technology Enablers – Back-Side Illumination (BSI)

3

Back-Side Illumination (BSI) (first seen in products 2009)

- Disruptive technology!
- "Removes" the metal wiring part from the "optical stack"
- Completely eliminates cross-talk in the BEOL (metal wiring)

Pixel sizes ~2um
- Eliminates BEOL cross-talk
- Easier metal routing



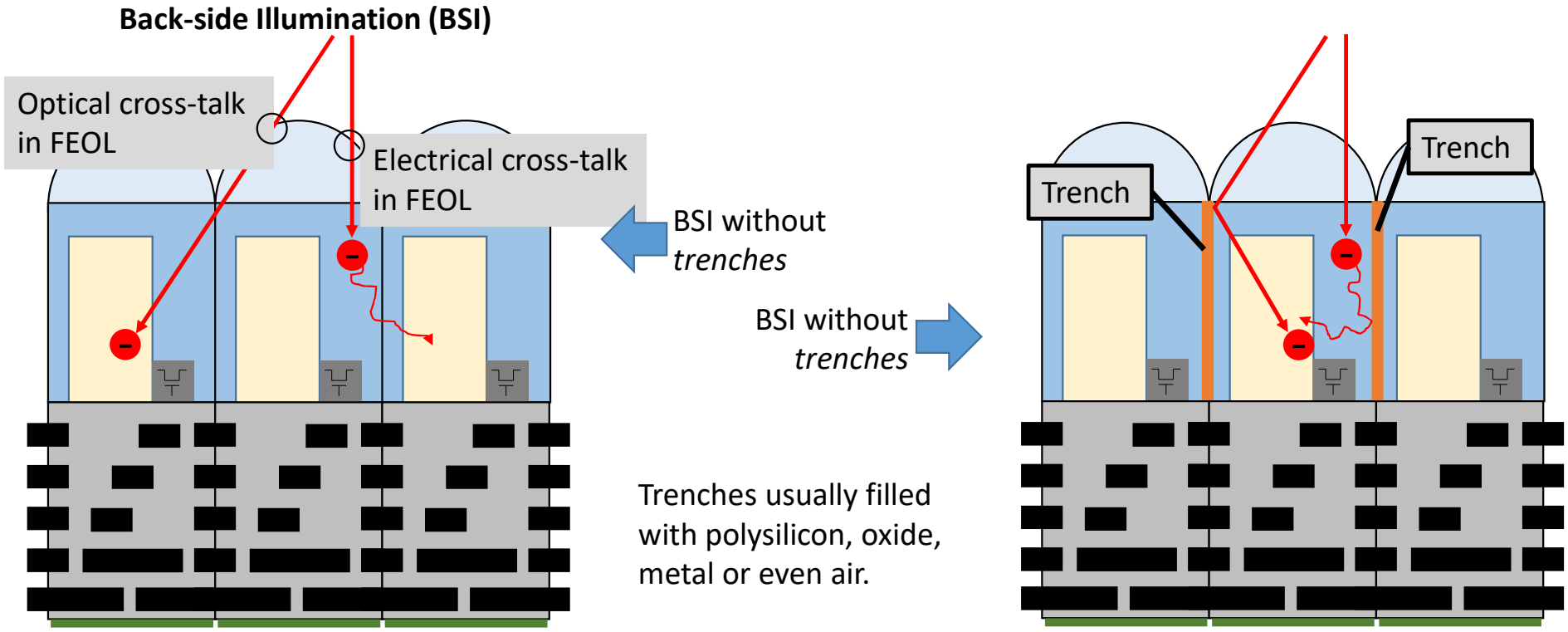
CIS Technology Enablers – Deep Trench Isolation (DTI)

Pixel sizes ~1-2um
- Less cross-talk in FEOL

4

Deep Trench Isolation (DTI) (first seen in products 2010)

- A technique to avoid electrical and optical cross-talk in the silicon bulk (FEOL)
- Back-Side-Illumination (BSI) was a disruptive technology, but it was not until DTI the benefits were fully utilized!



CIS Technology Enablers – Vertical Transfer Gate (VTG)

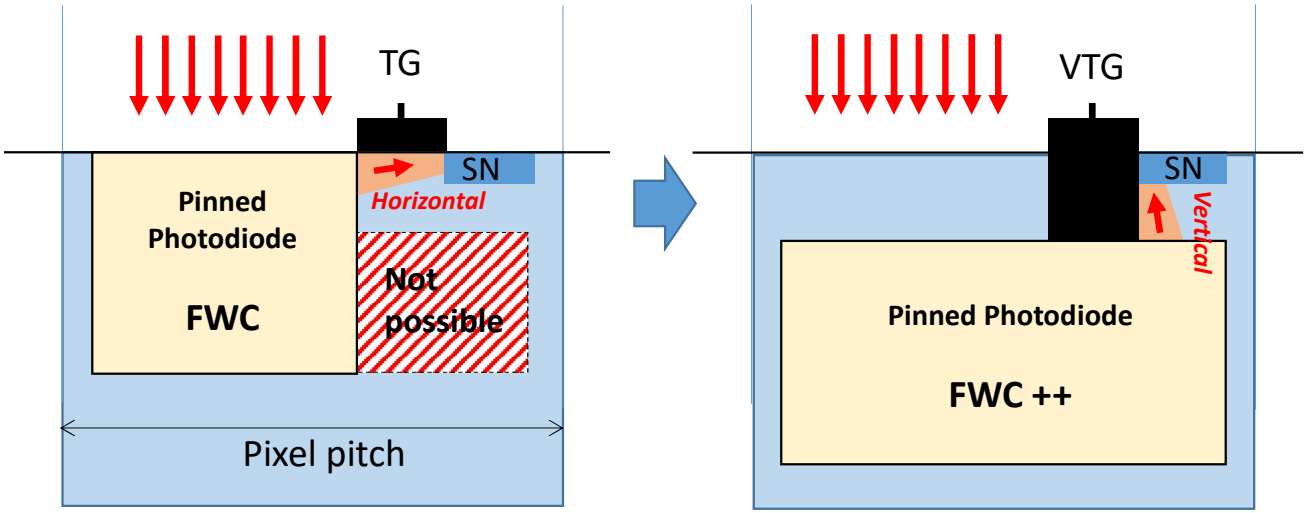
Pixel sizes ~1um
- Increases the FWC

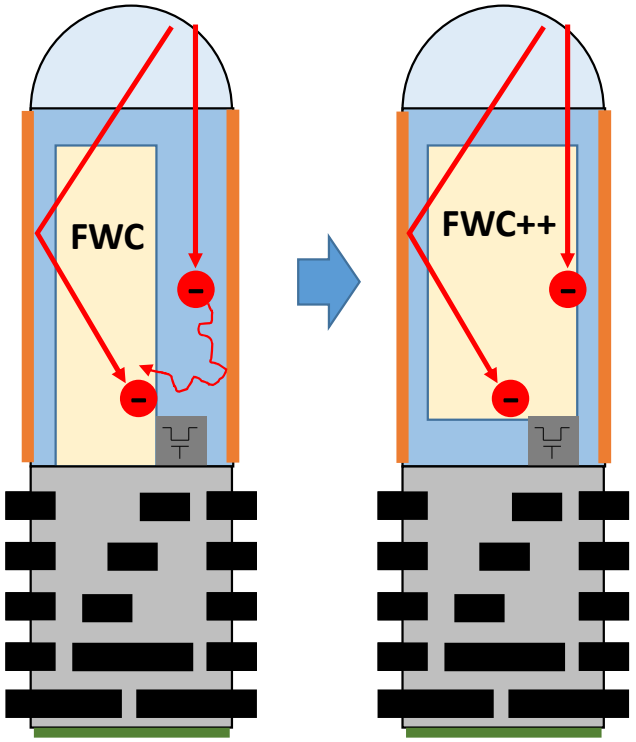
5

Vertical Transfer Gate (VTG) (first seen in products 2013)

- To improve the Full Well Capacity (FWC) (improved image quality) for small pixels a so called Vertical Transfer Gate (VTG) can be used
- Part of the pixel area is occupied by transistors, e.g. the transfer gate transistor …and this results in that less space is available for the pinned photodiode (PPD)

- The VTG buries the photo diode under the transistors



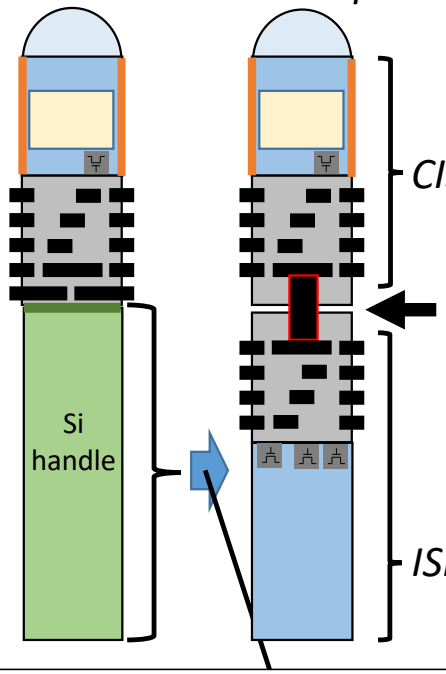


Pixel sizes ~0.8um
- Higher degree of integration

6

3D Stacking (first seen in CIS Smartphone products 2018)

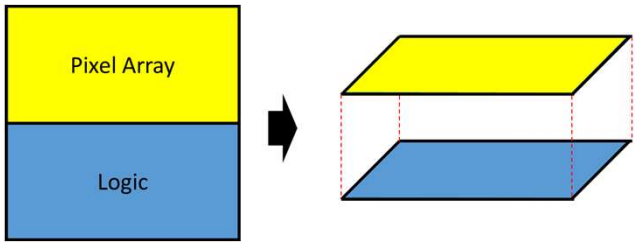
- Disruptive technology!
- 3D stacking is not reducing cross-talk or full well capacity, rather offering more computational performance *in the same package*!



Two main connection technologies:
- Through Silicon Vias (TSV)
- Cu-Cu Direct Bond Interconnect (DBI)

(Record: 1.4um pitch => 1um)

Replace the Si-handle with an "Image Signal Processor" (ISP) chip!



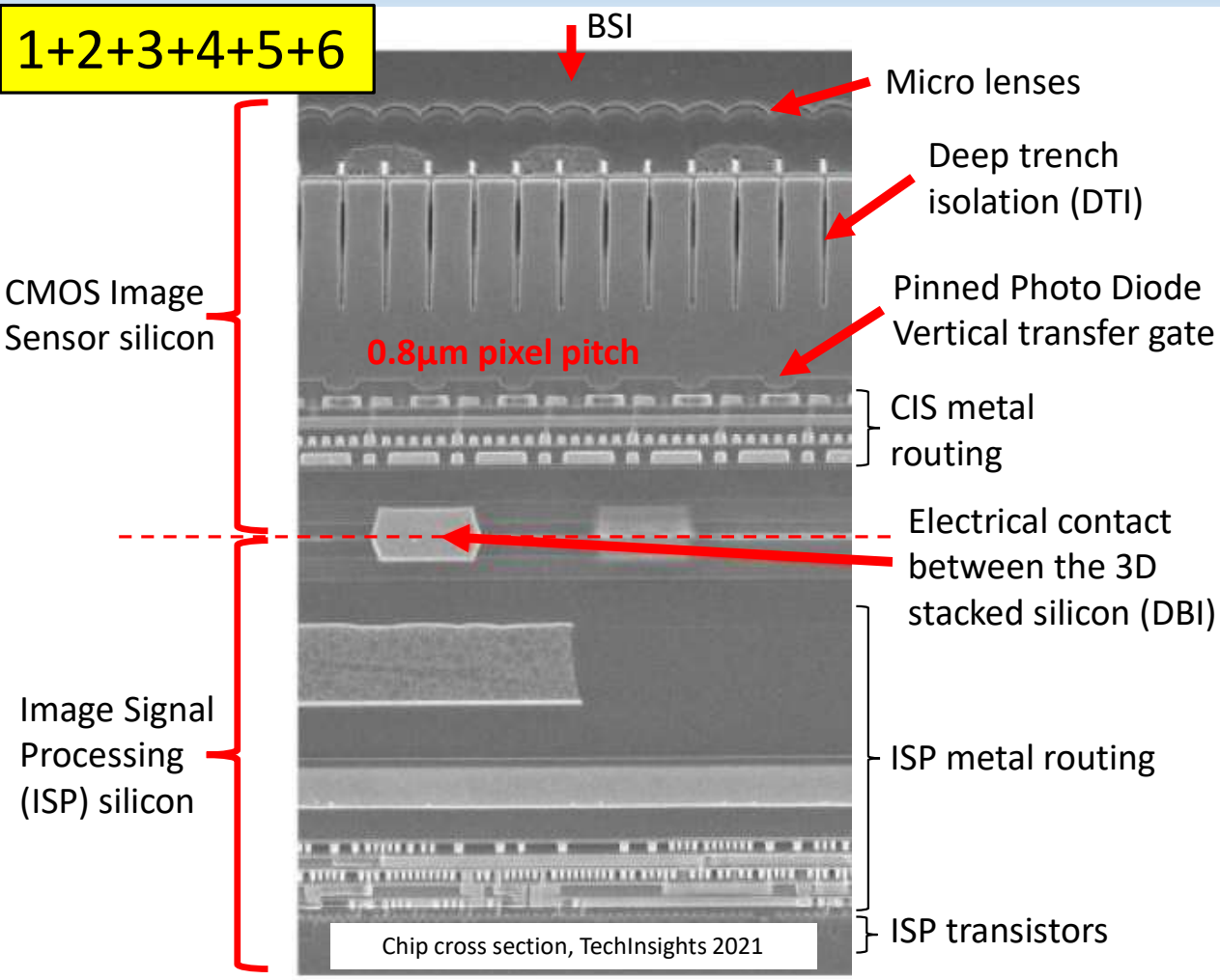
What to use the "extra" computational performance for?
- *Phase Detection Autofocus* (PDAF)
- *Remosaicing* for color images
- *Computational photography*
- *HDR* modes
- *Different advanced corrections* (noise filtering, pixel defects, …)
- …or detecting laser peaks in columns

SICK
Sensor Intelligence.

CMOS Image Sensors – Technology Evolution

CIS Technology Enablers – all bells and whistles!

1+2+3+4+5+6



For an Industrial CMOS image sensor pixel size is typically 6-3µm

All the technologies presented is useful and now available to a reasonable cost for Industrial image sensors, despite the "low" volumes.

The exception is the VTG that is really not necessary for pixels larger than ~1µm.

SICK
Sensor Intelligence.

Questions?

Summary:

- SICK uses CIS with on-chip intelligence to build one of the worlds fastest laser triangulation cameras
- CIS market is today dominated by Smartphone cameras and by Asian companies
- The CIS technology driver has been high-quality small pixels
- Six key CIS technologies was presented; uL, PPD, BSI, DTI, VTG, 3D Stacking

END

SICK
Sensor Intelligence.