LiU Guest Lecture

TSBB21 Computational Photography

SICK
Sensor Intelligence.

CMOS Image Sensor Technology

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Who am I?

- Johan Melander
  - 1995: MSc. Computer Science and Electrical Engineering, LiU
  - 1997: Lic. Eng. from Department of Electrical Engineering, LiU

  - 1997 I started at the LiU spin-off *Integrated Vison Products AB* (IVP AB) designing CMOS image sensors
    - IVP AB was founded 1985 by Robert Forchheimer and Anders Ödmark. IVP's core technology was their custom made CMOS image sensors.

  - 2003 IVP AB was fully integrated into the German industrial sensor company SICK AG (~12.000 employees, ~2.3B EUR sales), where we now represent SICK's *Innovation Center for Machine Vision*.
  - At *SICK IVP AB*, the technical work I have done has mainly focused on CMOS image sensors.

CMOS image sensor (CIS) technology

- CIS are today everywhere…
- It's the dominating image sensor technology for visible light

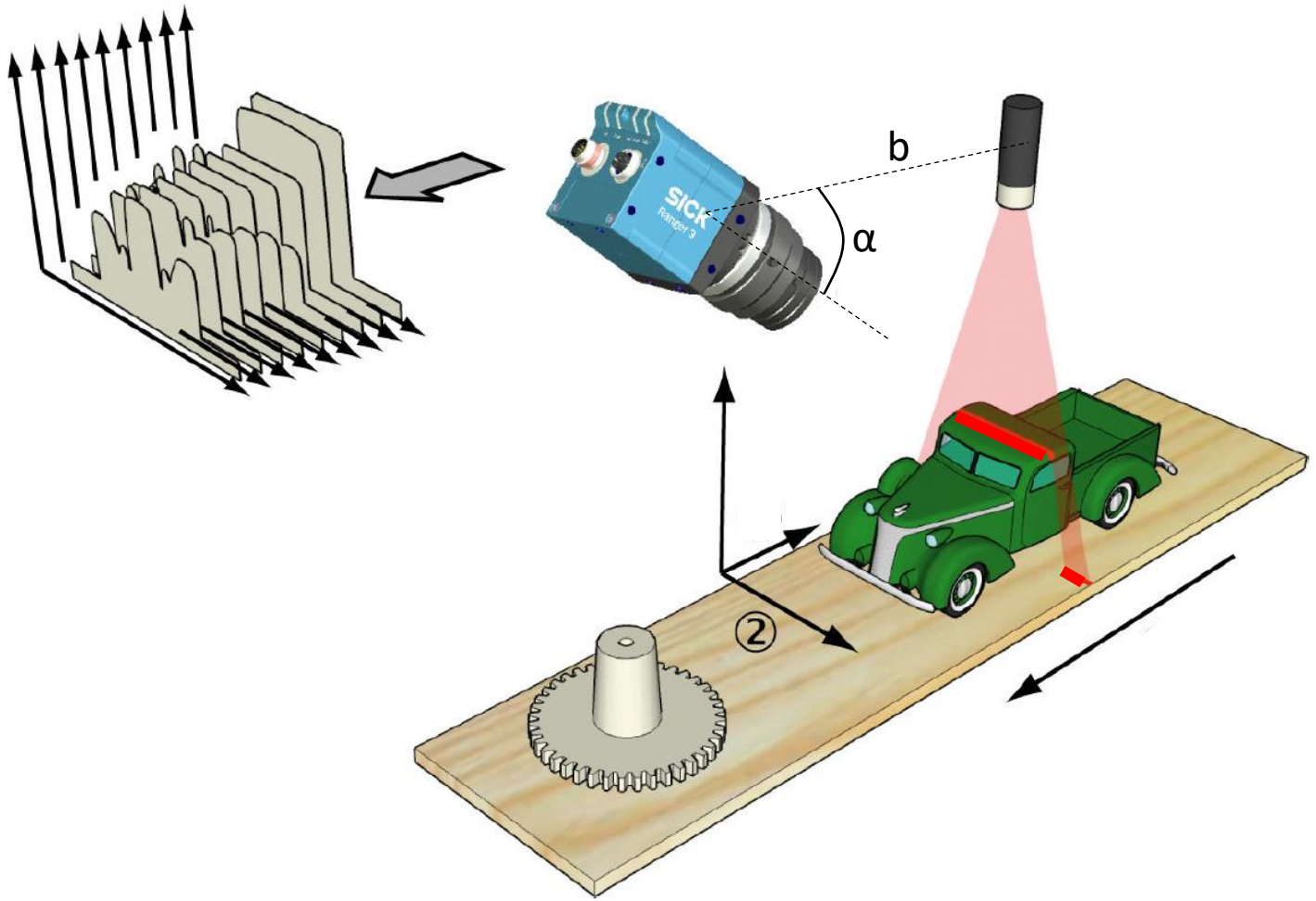
iPhone 16 Pro Max

- It has also enabled SICK to build one of the world's fastest laser triangulation sensors

Why do we work with CMOS image sensors at SICK?

Why do we work with CMOS image sensors at SICK?

At SICK (among other tings) we develop 3D cameras for industrial automation applications.
For the SICK *Ranger*/*Ruler* products we use the **laser triangulation** principle to acquire **3D data**.



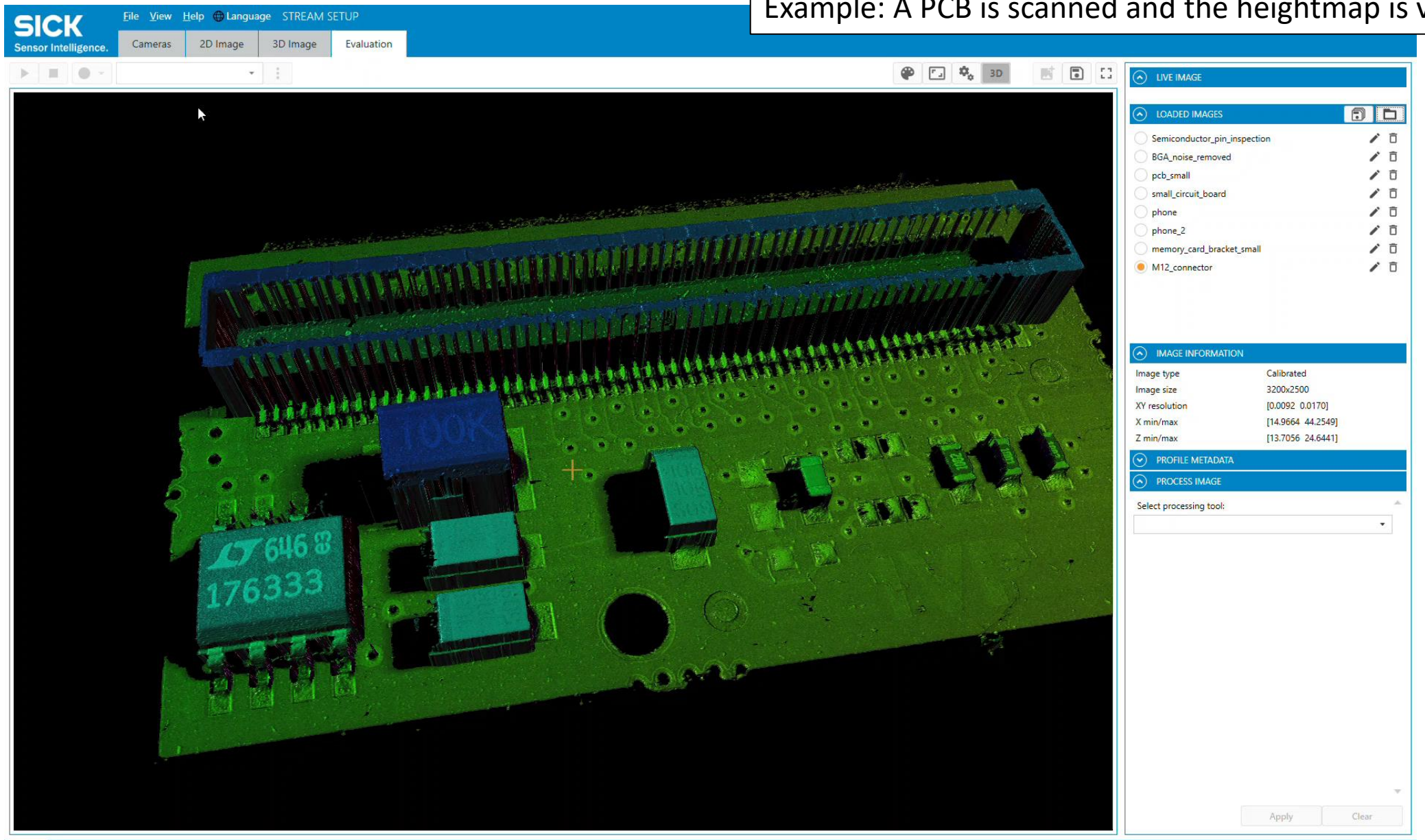
Laser Triangulation Principle

- A target is moving through a projected laser line.
- For each trigger a new image with laser line is acquired by the camera…
- … and given the “geometry” of the setup, the *height* (3D data) of the target in the laser plane can now be calculated
- H*eight profiles* are put together to form the complete 3D data (*height map*) of the object

CMOS Image Sensor Technology

Why do we work with CMOS image sensors at SICK?

Example: A PCB is scanned and the heightmap is viewed in a 3D viewer



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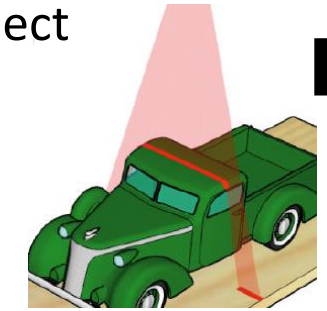
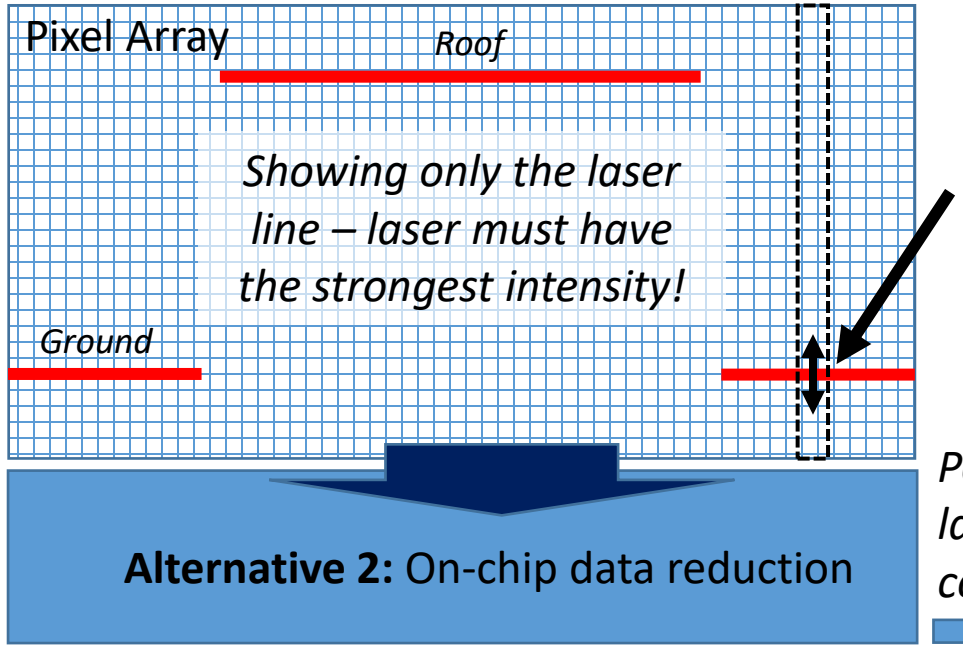
Why do we work with CMOS image sensors at SICK?

And that is why I work with custom CMOS image sensors at SICK

The image sensor in the laser triangulation camera "sees" the laser profile projected on the object





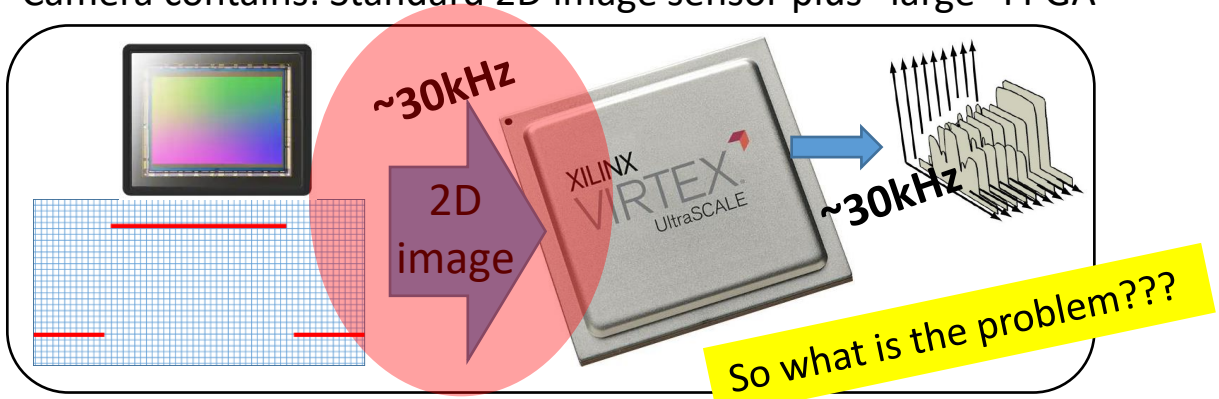
The position of the laser line in a column of the image sensor is proportional to the height of the object (3D information)

Position of laser in each column

This enables us to do the fastest and most compact laser triangulation systems in the world

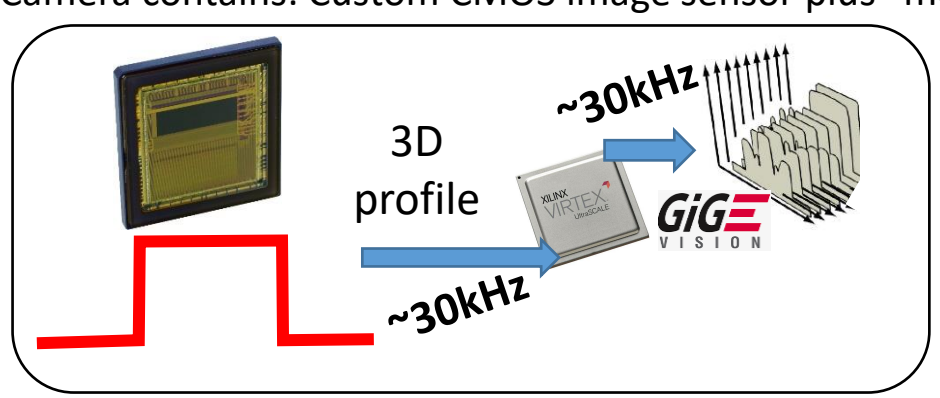
Alternative 1 – "Brute force"

Camera contains: Standard 2D image sensor plus "large" FPGA



Alternative 2 – "SICK approach"

Camera contains: Custom CMOS image sensor plus "medium" FPGA

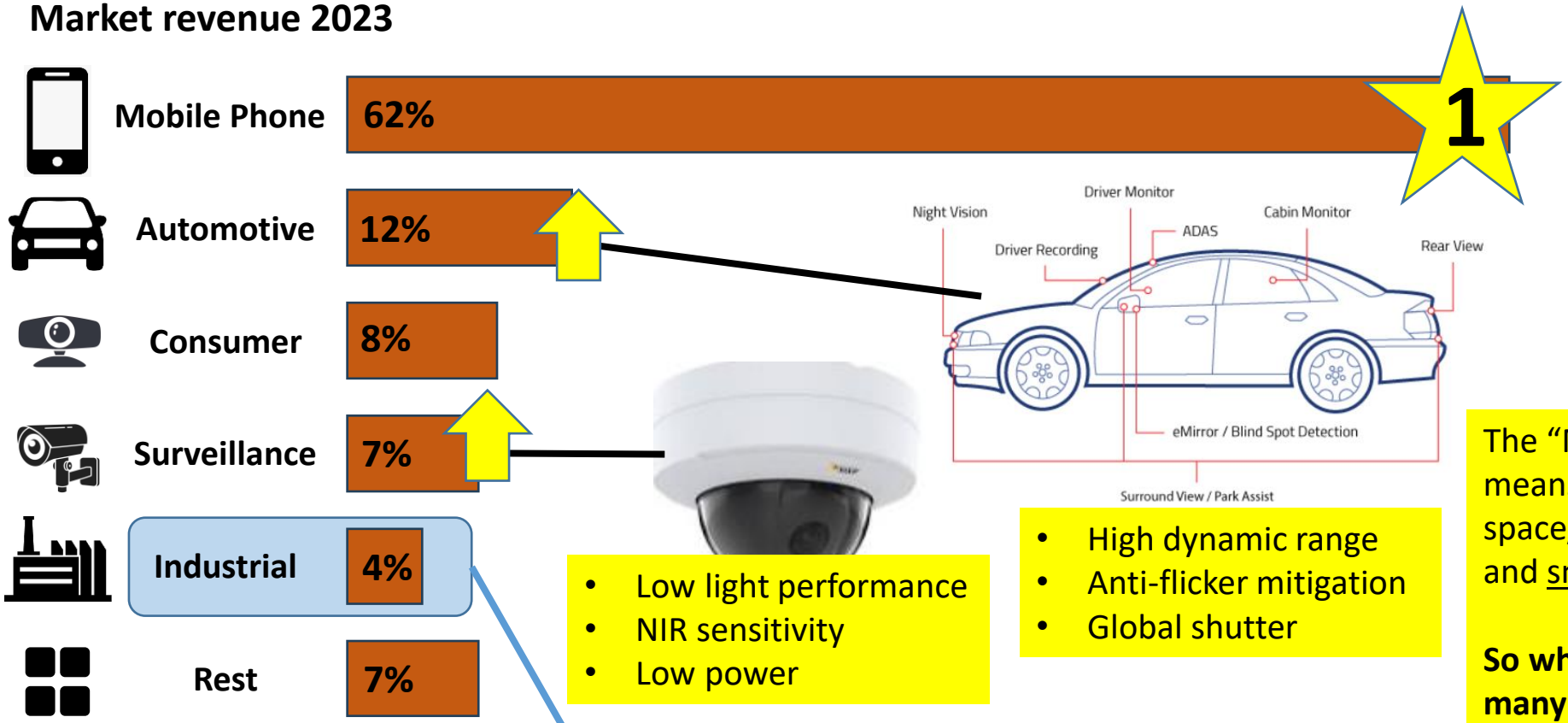


SICK Sensor Intelligence.

What is driving the technology evolution of CMOS image sensors?

CMOS Image Sensor Technology
What is driving the technology evolution

CMOS Image Sensor (CIS) where are they used?
Market revenue 2023



- Low light performance
- NIR sensitivity
- Low power

- High dynamic range
- Anti-flicker mitigation
- Global shutter

iPhone 16 Pro Max

The “Megapixel race” for Smartphones means higher resolution imagers in the same space/volume => and this leads to smaller and smaller pixels.

So what has propelled the CIS technology for many years is the need for high quality small pixels.

Today’s smallest pixel:
- *Samsung*: 200Mpix, 0.56µm pixel size (2024)
- *Omnivision:* 200Mpix, 0.56µm pixel size (2023)

Source: TechInsights

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For CMOS imagers we today (since the mid 90:s) need a specialized semiconductor process – why?

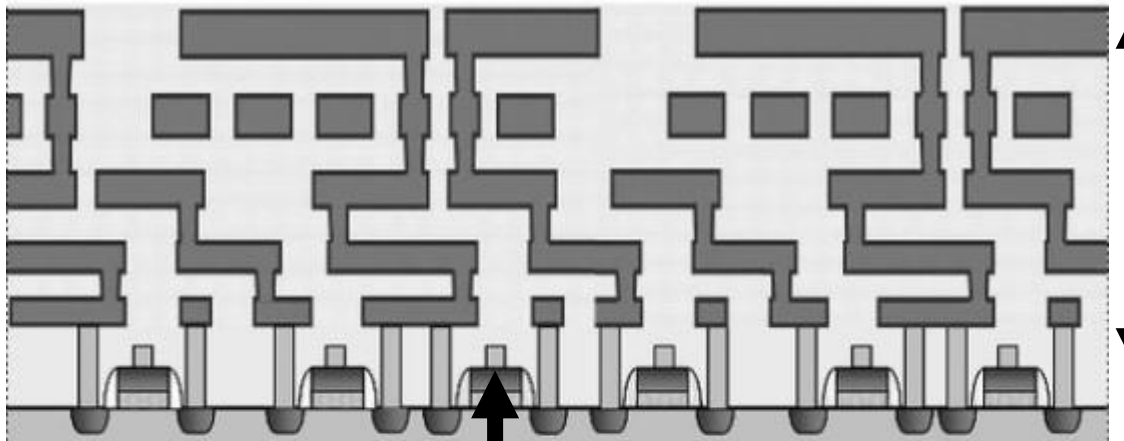
Why a specialized CMOS manufacturing process?

A **standard CMOS process** is used to manufacture e.g. the Apple M4 CPU or an Intel Core CPU.

- Process is optimized for *logic*
- Scaling to smaller geometries and higher performance still follows *"Moore's law"*
- Today, state of the art *process nodes* are at 3nm-5nm
  (2024; Apples M4, 28B trans, TSMC 3nm)

Frontside

Chip cross-section



Back-end-of-line (BEOL)

- Metal wiring and interconnects

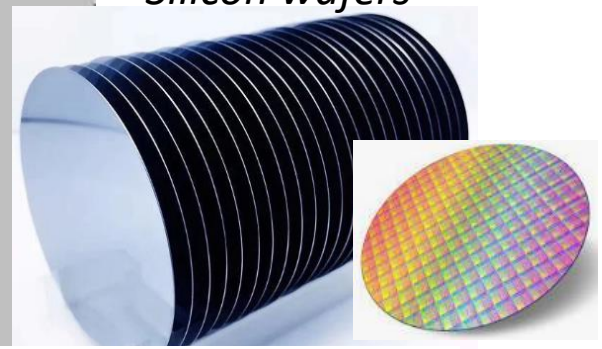
Front-end-of-line (FEOL)

- The silicon where you do your Devices; Transistors, diodes, etc.

https://www.researchgate.net/figure/Schematic-cross-section-of-a-part-of-an-integrated-circuit-illustrating-transistors_fig1_283906716

Backside

Silicon wafers



https://www.msesupplies.com/products/mse-pro-1-cassette-qty-25-of-100-mm-p-type-b-doped-prime-grade-silicon-wafer-100-ssp-10-20-ohm-cm?variant=23715278815290

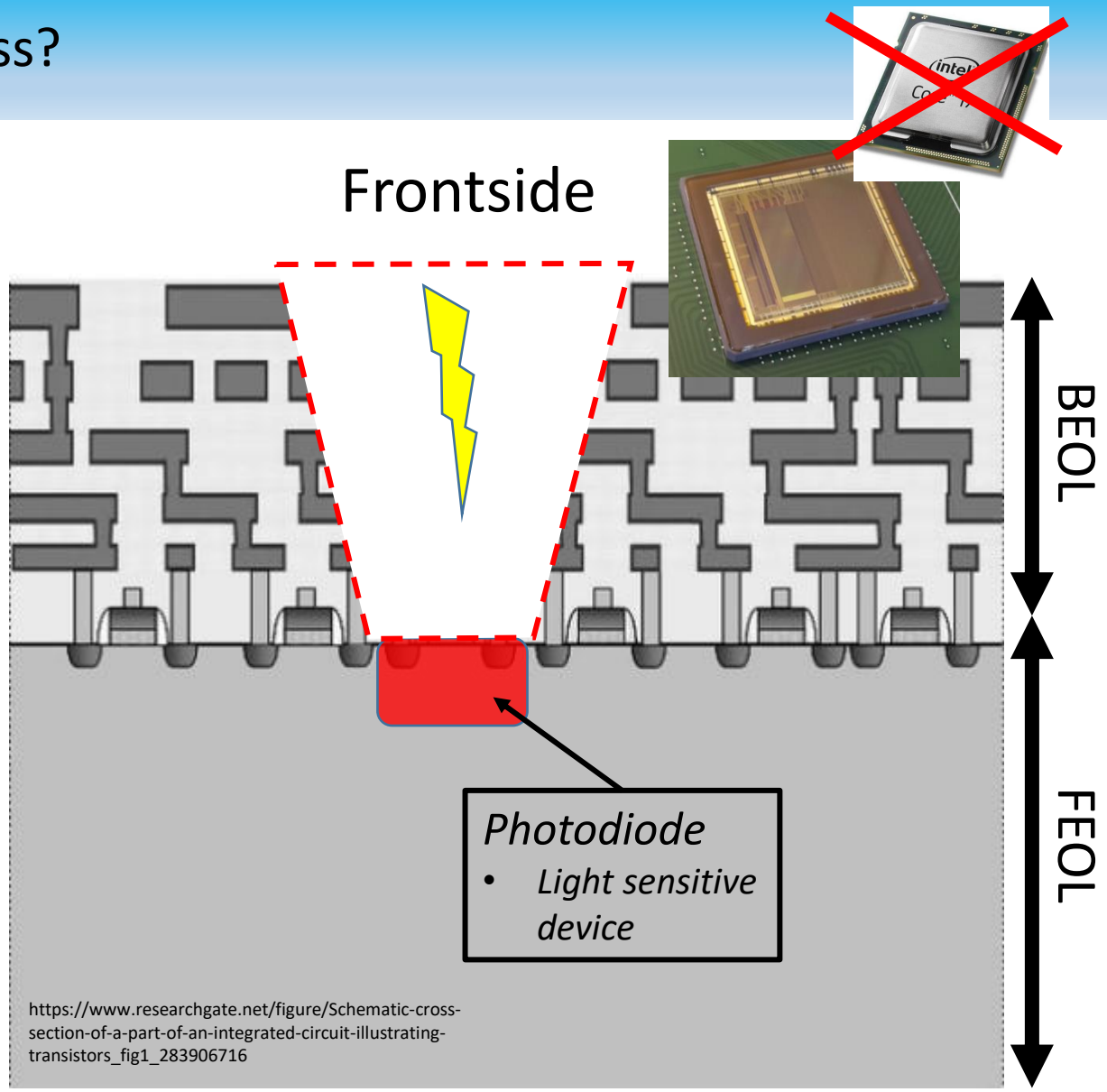
Why a specialized CMOS manufacturing process?

A CMOS Image Sensor (*CIS*) process is very similar to a CMOS process, but …

… today contains **highly specialized process steps** in order to make good optical detection possible (since mid 90's).

First obvious things (not needing a specialize process)are that you need a good photo sensitive device (photodiode)
…
… and that you cannot route any wires on top of the pixel
… and need a glass lid on top of the package!

So, besides that, what else is needed in a modern CIS process?

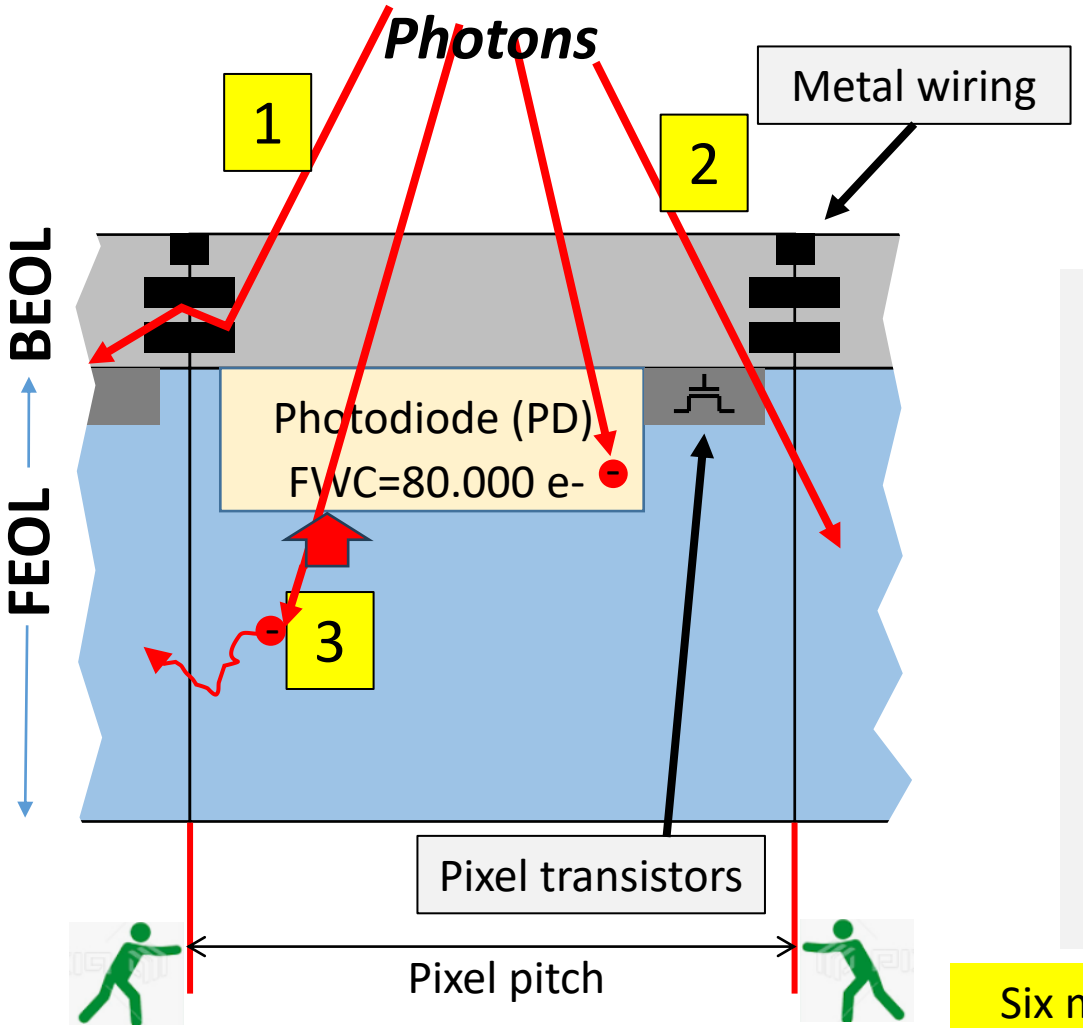


CIS technology enablers

…the 6 most important

CIS Technology Enablers – *Cross-talk* and *Full Well Capacity* (FWC)

First, two key terms: *Cross-talk* and *Full Well Capacity* (FWC)



1. Optical cross-talk in the BEOL
2. Optical cross-talk in the FEOL
3. Electrical cross-talk in the FEOL

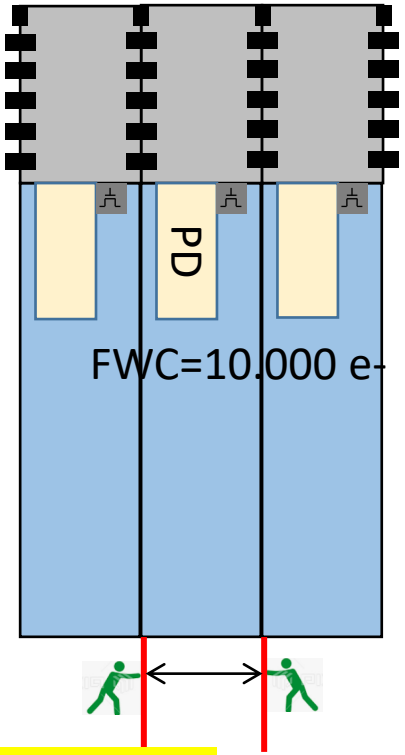
If you just take the next technology node and shrink the pixel;

- Photodiode Full Well Capacity (FWC) decreases => *poorer image quality*
- Cross-talk has a higher relative impact => *poorer image quality*

… so the enablers for a CIS process supporting **high-quality small pixels** boils down to;

1. Maintain a good enough FWC and …
2. … reduce the cross-talk

Small pixels in a modern technology



Six most important technologies to achieve this will now follow!

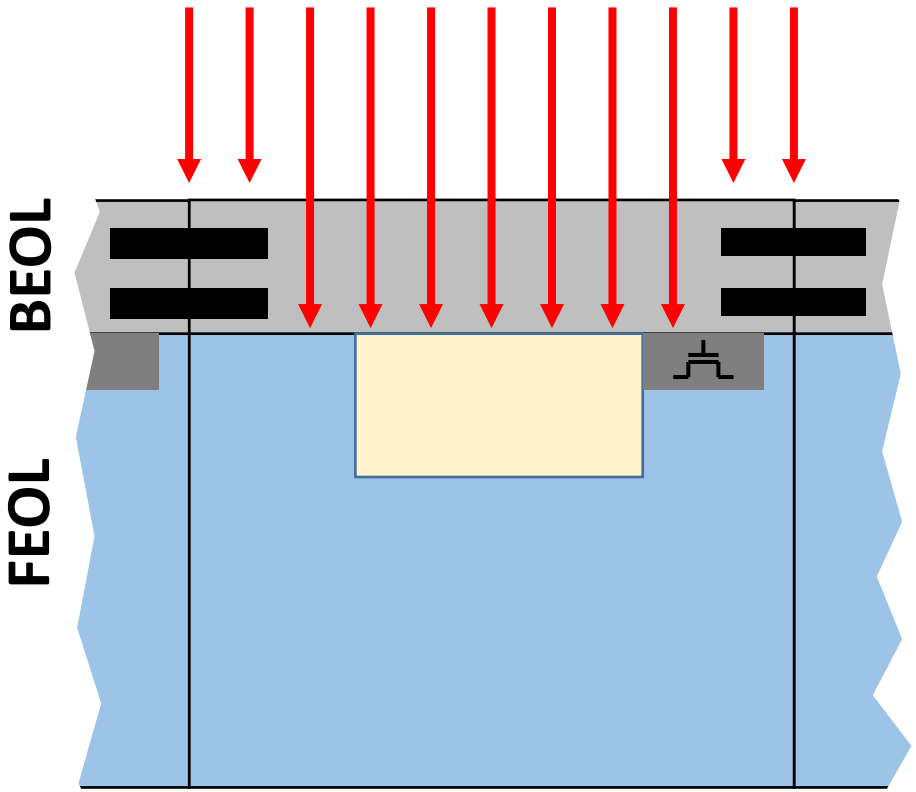
CIS Technology Enablers – Micro Lenses

Intro: Pixel sizes >10um
- Reduced cross-talk
- “Less light is wasted”

1

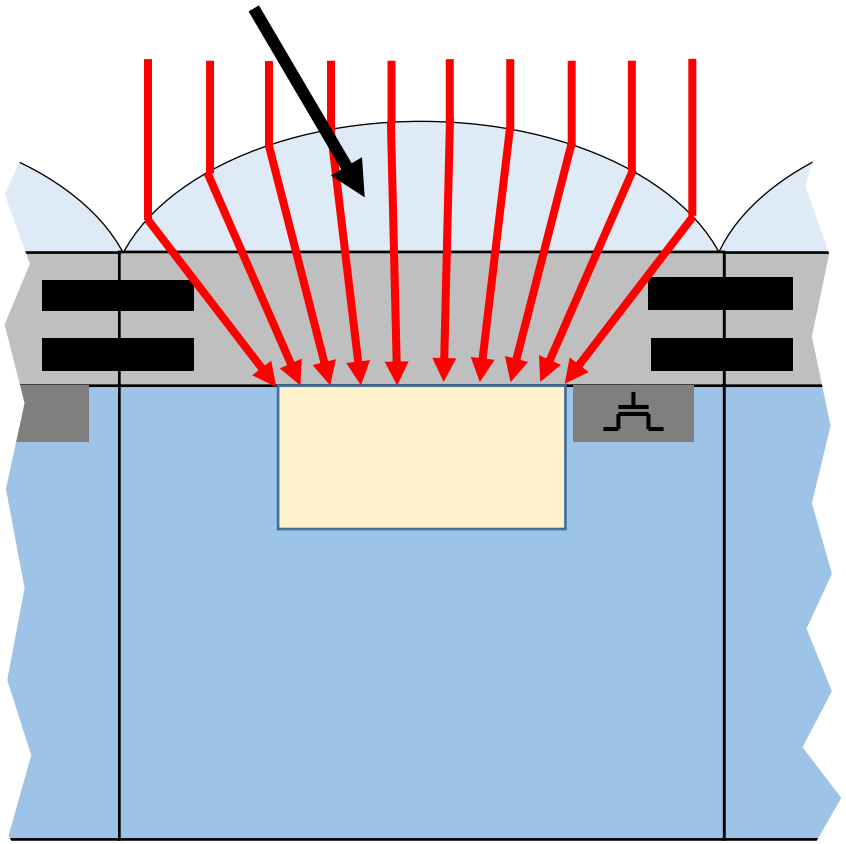
Micro lenses (already in the early 90’s)

- Focus the light (photons) to find its way to the photodiode



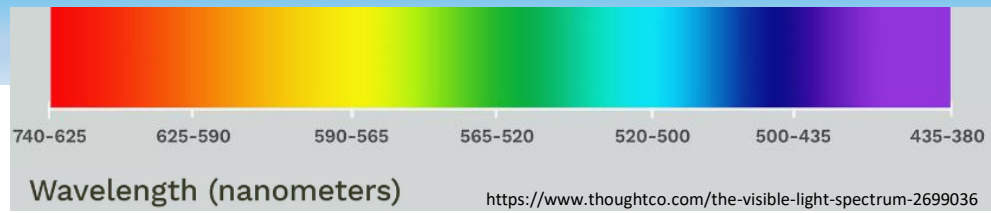
Put *micro lenses* on top of the pixel to direct a “larger portion” of the incoming photons to the photodiode.

Micro lense. Applied after BEOL in a special post-processing step.



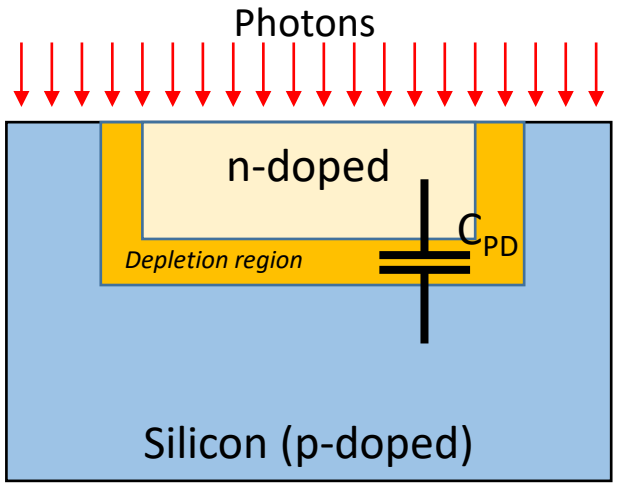
CIS Technology Enablers – The Pinned PhotoDiode, PPD

2a



How do we detect light? The *standard* photodiode!

- Light is a stream of photons (at least in this context)…
- A single photon has an energy that depends on its wave length, λ (color) – $E_{Ph}=h*c/\lambda$ (c=speed of light, h=Planck's constant)
- If the single photon energy is *higher than the bandgap of silicon* ($E_{g,Si}$=1.12eV) it can "set one electron free" in the silicon (excite it from the *valence band* to the *conduction band*)
- If we collect all *photo generated electrons* during the *exposure time* we can get an "electric measure" of the *intensity of light* during the exposure time
- That is, we need an *electronic device* that can collect/register the photogenerated electrons
- First device used in CIS was the "*photodiode*" – a *PN-junction* in the silicon (FEOL) acting as a light sensitive capacitor



Operation of a standard photodiode:

1. Precharge the PN-junction capacitance to a fix voltage, e.g. 3.3V
2. The photogenerated electrons will discharge the PN-junction capacitance during the exposure time
3. At the end of the exposure time, the voltage across the PN-junction capacitance will be proportional to the intensity of light during exposure

Drawbacks with a photodiode:

1. Relatively high *dark noise*
2. Difficult to make a low noise *readout*
3. Difficult to tune *image performance*

CIS Technology Enablers – The Pinned PhotoDiode, PPD

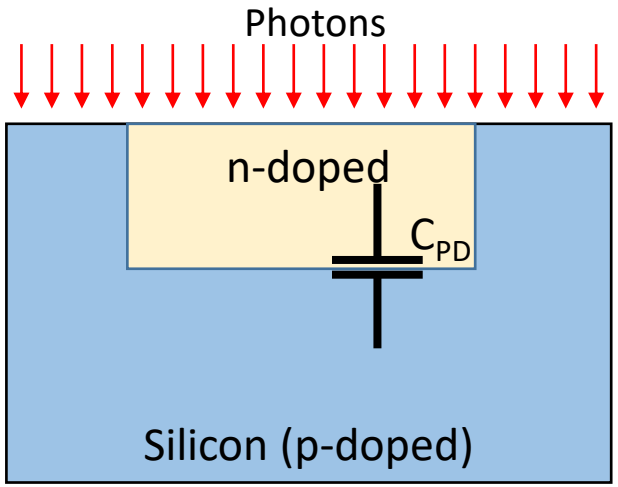
2b

Intro: Pixel sizes ~10um
- In general a lower noise pixel => maintained image quality with lower FWC

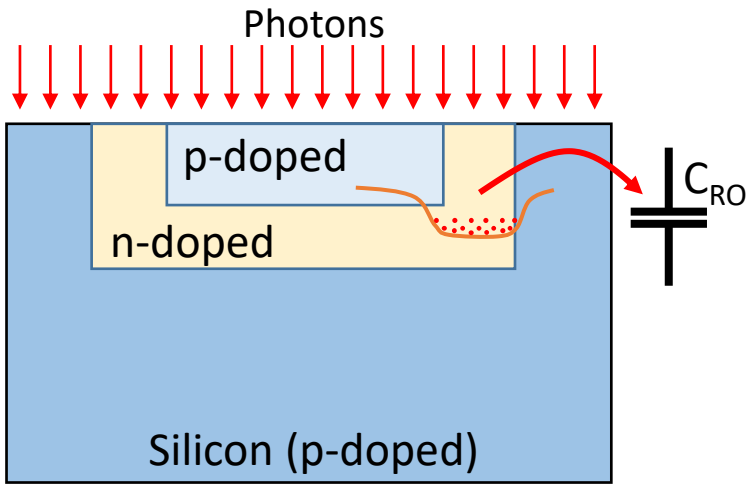
The *pinned* photodiode!

- In 1995 the Pinned PhotoDiode (PPD) was first used in CIS
  - Maybe the most important invention for CIS
  - A device structure for collecting photogenerated charges inherited from CCD image sensors
- Alleviates all the drawbacks of the standard photodiode
  - Requires very special process steps

Standard photodiode



Pinned photodiode



The pnp-structure creates a potential *well* where photogenerated electron can be collected.

Operation of a pinned photodiode:
1. Clear/reset the *well*
2. Collect electrons in the well during exposure time
3. Transfer the charges in the well to a readout capacitor – i.e. converting charge to voltage
4. The voltage on the readout capacitor will now be proportional to the intensity of light during exposure

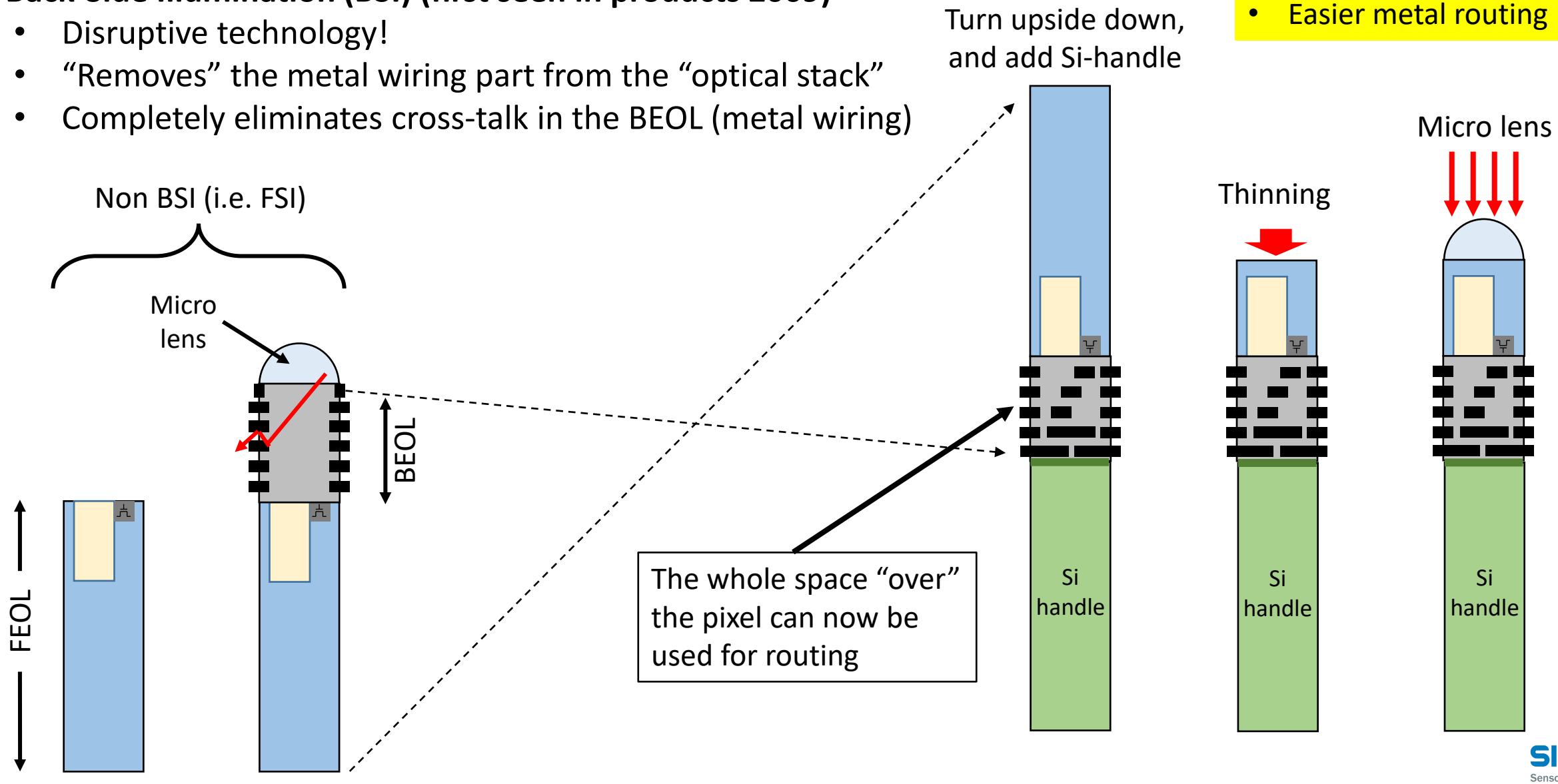
CIS Technology Enablers – Back-Side Illumination (BSI)

3

Intro: Pixel sizes ~2um
- Eliminates BEOL cross-talk
- Easier metal routing

Back-Side Illumination (BSI) (first seen in products 2009)

- Disruptive technology!
- "Removes" the metal wiring part from the "optical stack"
- Completely eliminates cross-talk in the BEOL (metal wiring)



CIS Technology Enablers – Deep Trench Isolation (DTI)

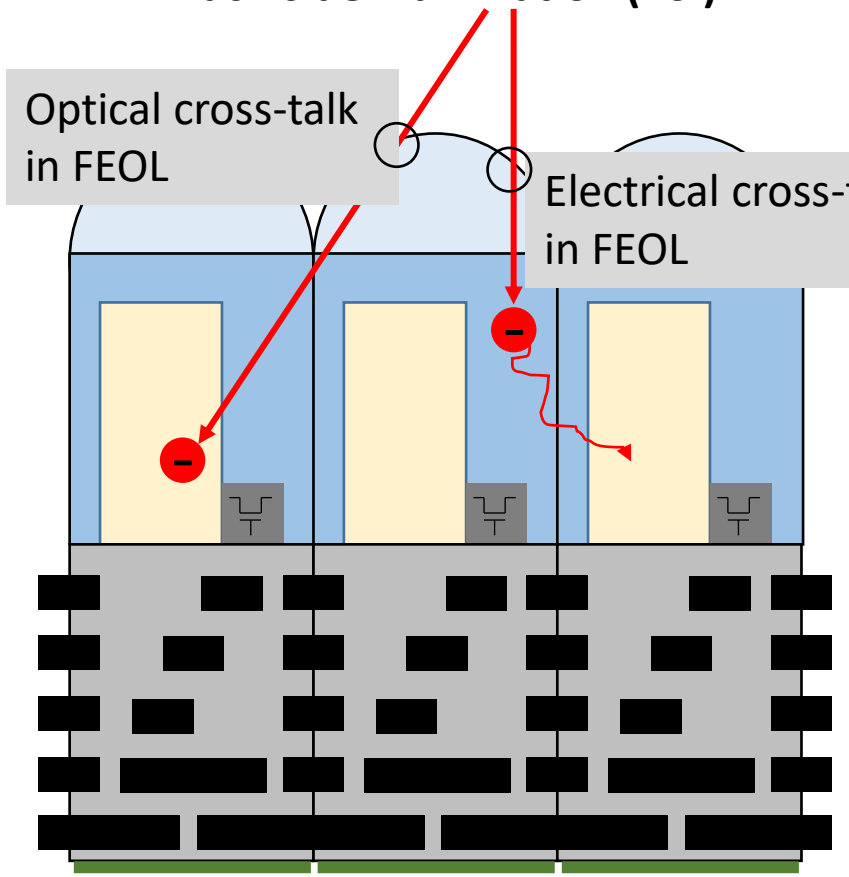
Intro: Pixel sizes ~1-2um
- Less cross-talk in FEOL

4

Deep Trench Isolation (DTI) (first seen in products 2010)

- A technique to avoid electrical and optical cross-talk in the silicon bulk (FEOL)
- Back-Side-Illumination (BSI) was a disruptive technology, but it was not until DTI the benefits were fully utilized!

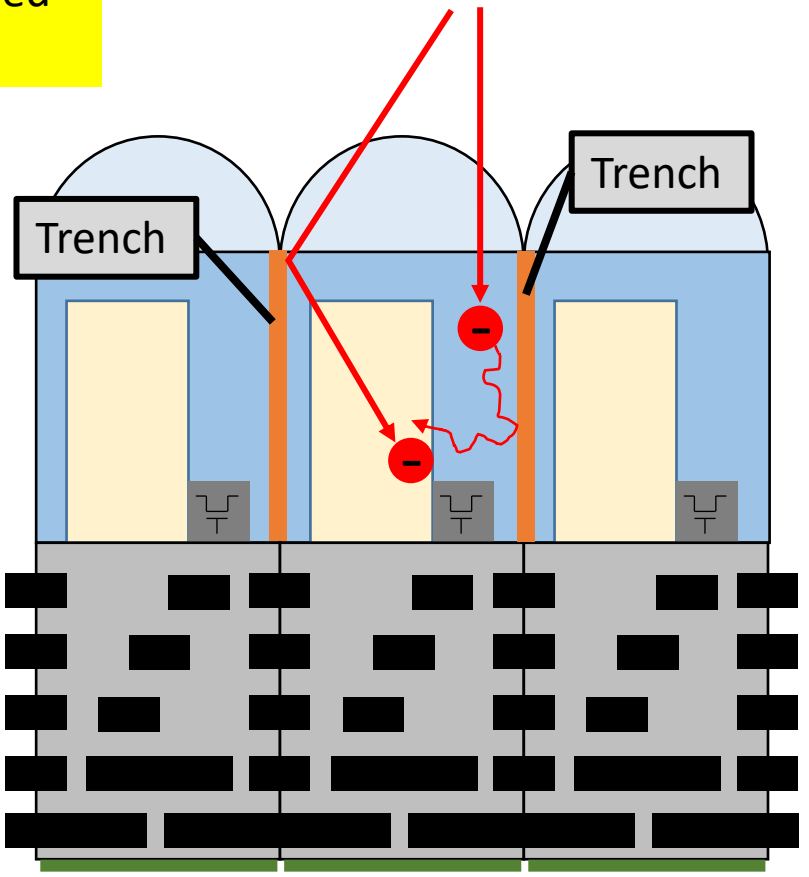
Back-side Illumination (BSI)



NOTE! We have now "removed" all cross-talk effects!

BSI without *trenches*

BSI without *trenches*



Trenches usually filled with polysilicon, oxide, metal or even air.

CIS Technology Enablers – Vertical Transfer Gate (VTG)

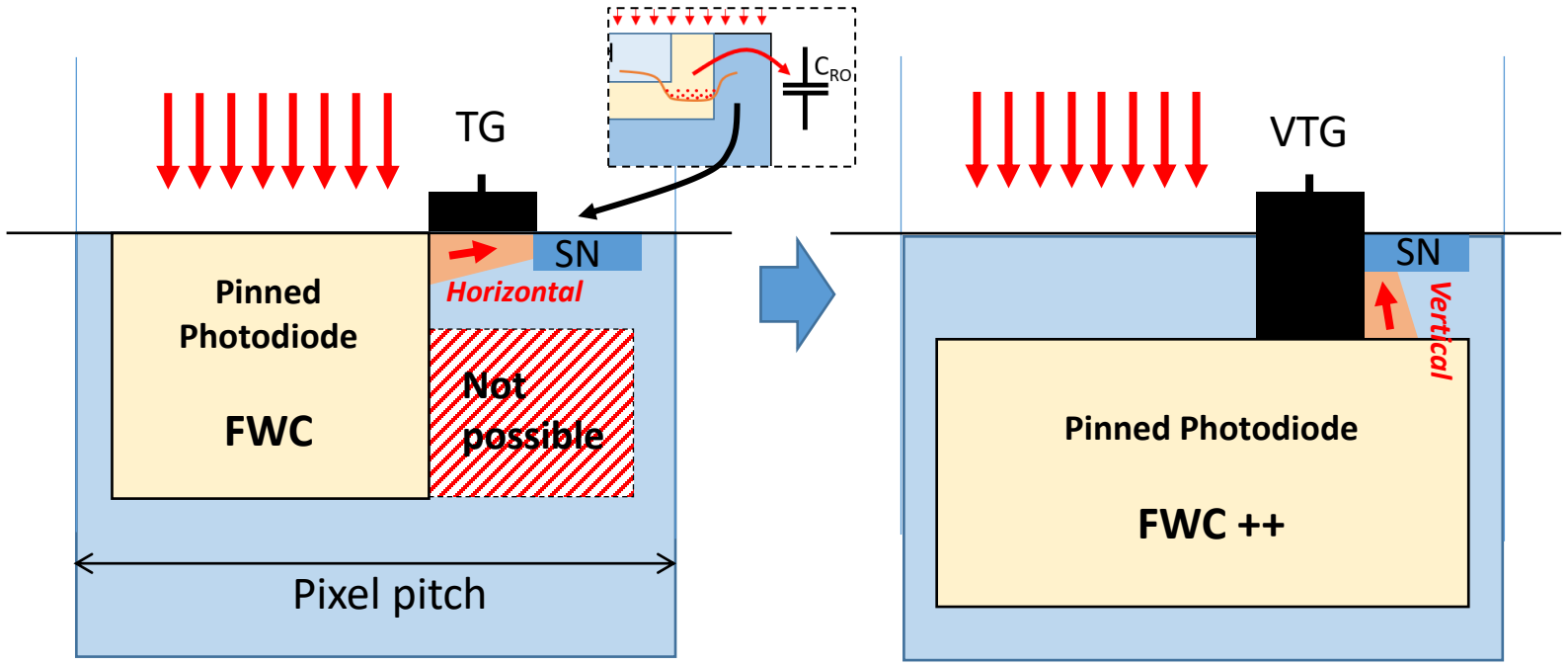
Intro: Pixel sizes ~1um
- Increases the FWC

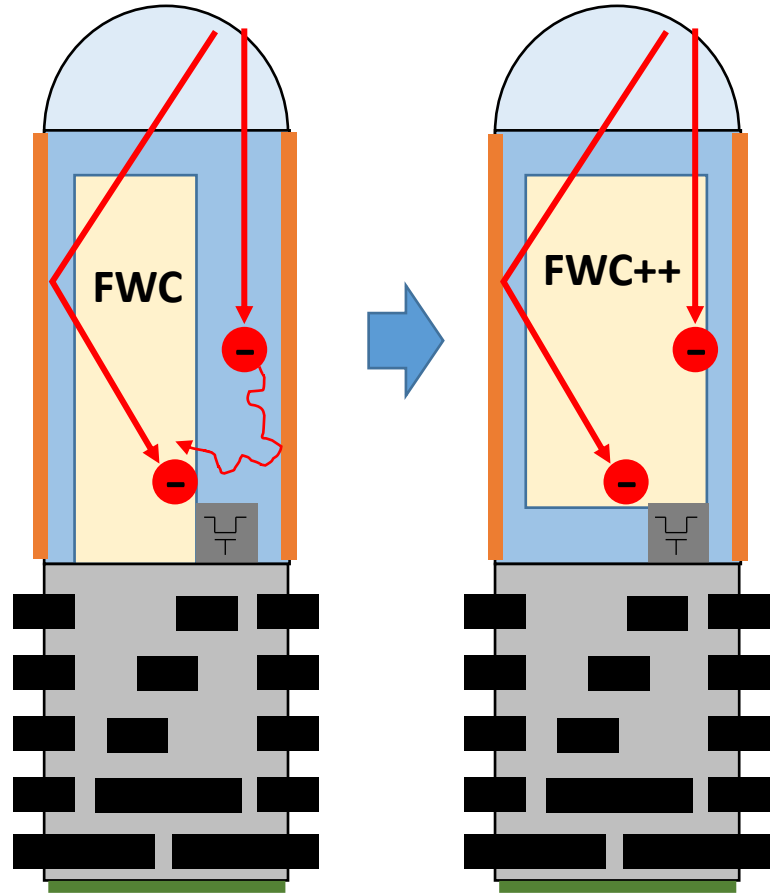
5

Vertical Transfer Gate (VTG) (first seen in products 2013)

- To improve the Full Well Capacity (FWC) (improved image quality) for small pixels a so called Vertical Transfer Gate (VTG) can be used
- Part of the pixel area is occupied by transistors, e.g. the transfer gate transistor …and this results in that less space is available for the pinned photodiode (PPD)

- The VTG buries the photodiode under the transistors



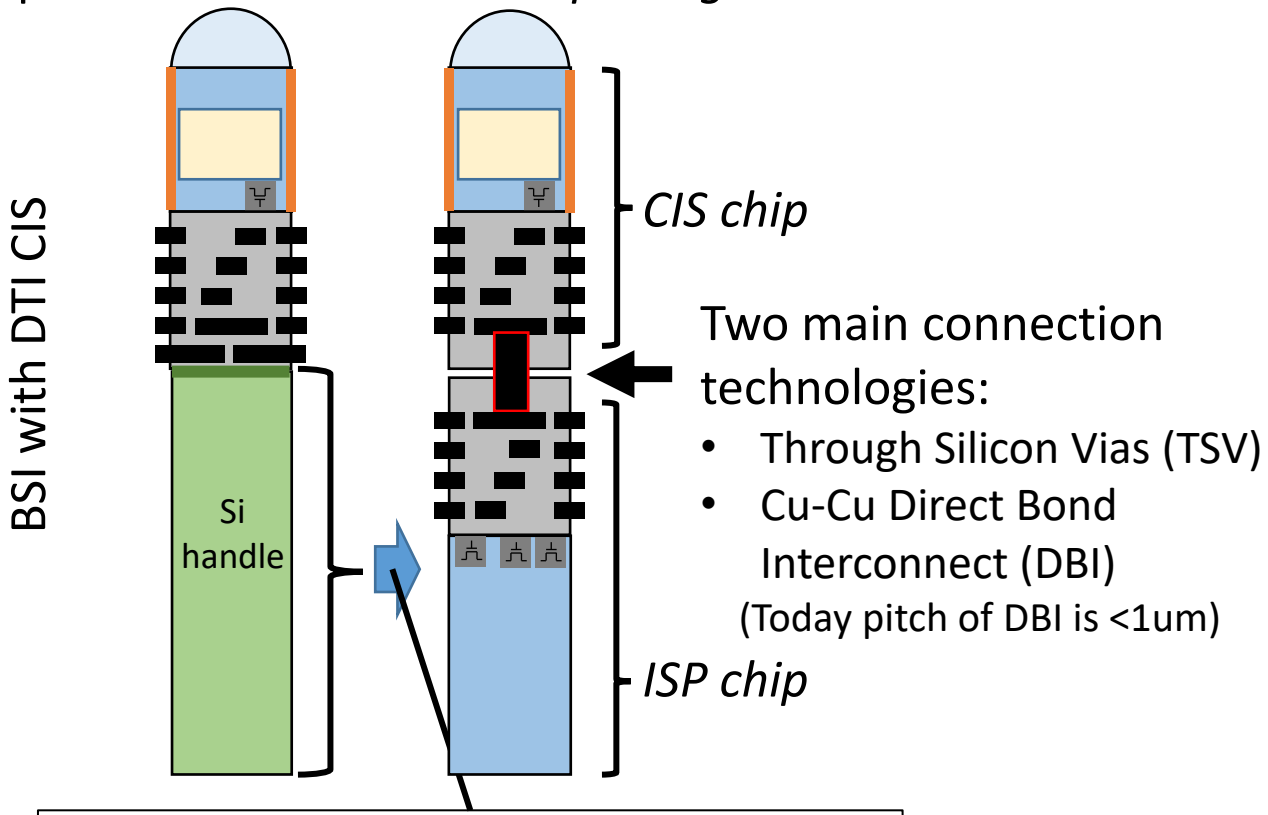


Intro: Pixel sizes ~0.8um
- Higher degree of integration

6

3D Stacking (first seen in CIS Smartphone products 2018)

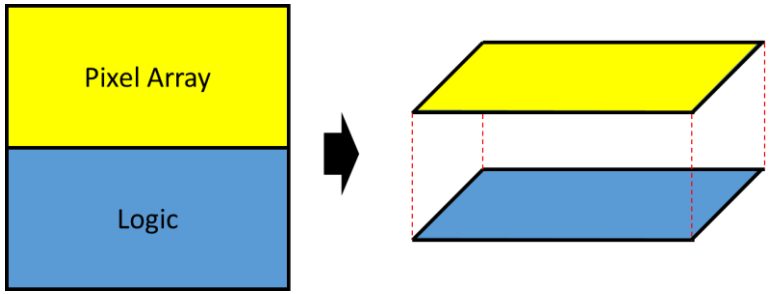
- Disruptive technology!
- 3D stacking is not reducing *cross-talk* or *full well capacity*, rather offering more computational performance *in the same package*!



Two main connection technologies:
- Through Silicon Vias (TSV)
- Cu-Cu Direct Bond Interconnect (DBI)

(Today pitch of DBI is <1um)

Replace the Si-handle with an "Image Signal Processor" (ISP) chip!

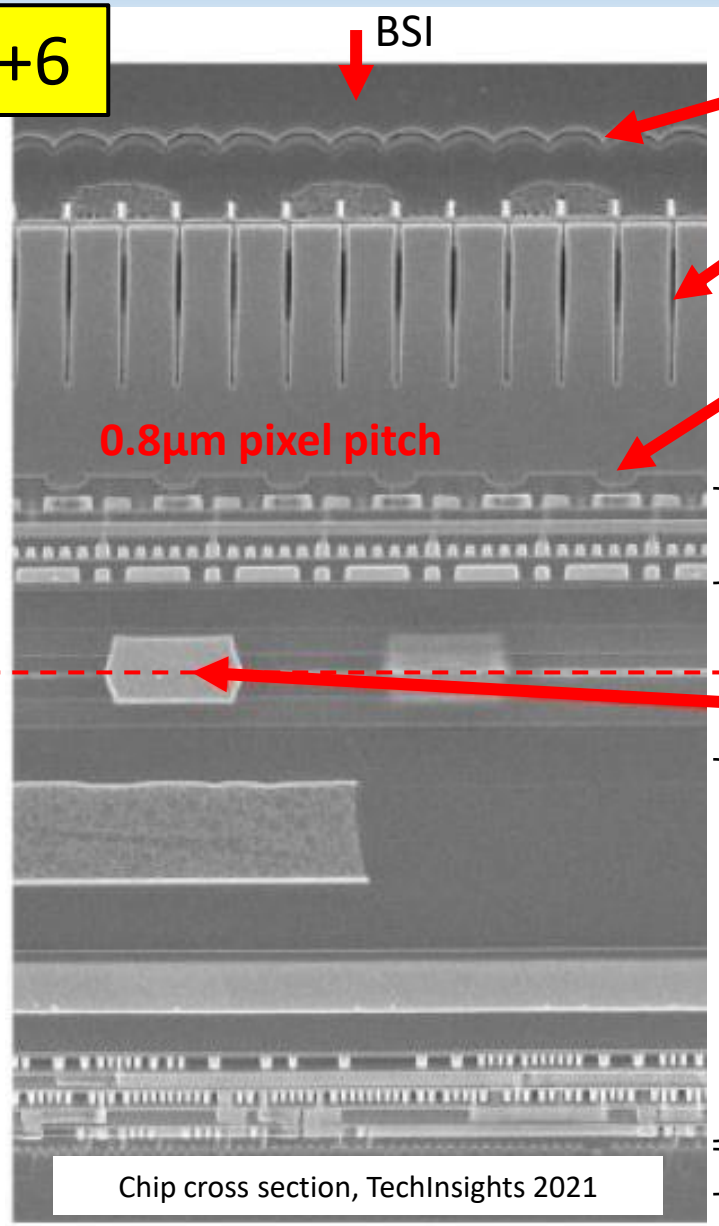


What to use the "extra" computational performance for?
- *Phase Detection Autofocus* (PDAF)
- *Remosaicing* for color images
- *Computational photography*
- *HDR* modes
- *Different advanced corrections* (noise filtering, pixel defects, …)
- …or detecting laser peaks in columns ;-)

CIS Technology Enablers – all bells and whistles!

1+2+3+4+5+6

SEM photo



For an Industrial CMOS image sensor pixel size is typically 6-3µm

All the technologies presented are useful and now available to a reasonable cost for Industrial image sensors, despite the "low" volumes.

The exception is the VTG that is really not necessary for pixels larger than ~1µm.

Questions?

Summary:

- SICK designs CIS with on-chip intelligence to build one of the worlds fastest laser triangulation cameras
- CIS market is today dominated by Smartphone cameras
- The CIS technology driver has until now been high-quality small pixels
- Six key CIS technologies was presented; uL, PPD, BSI, DTI, VTG, 3D Stacking

END

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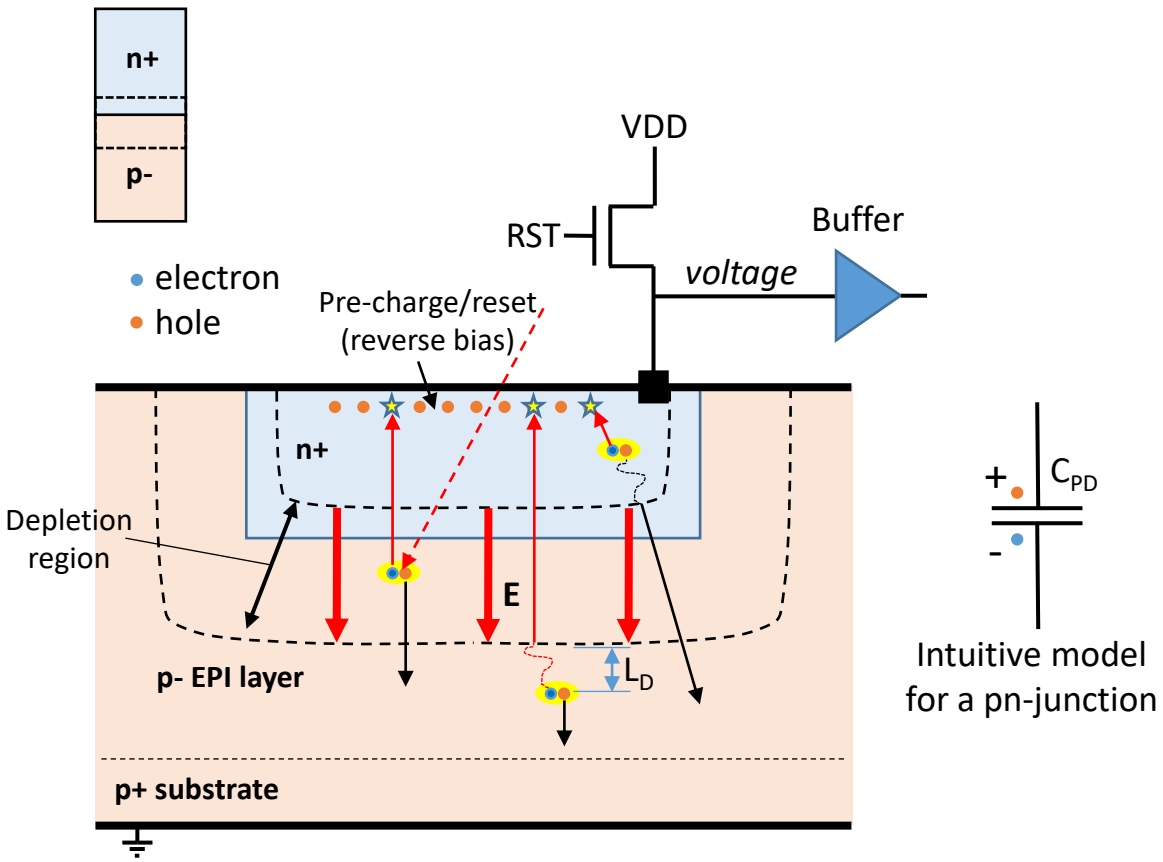
CIS Technology Enablers – The Pinned Photo Diode, PPD

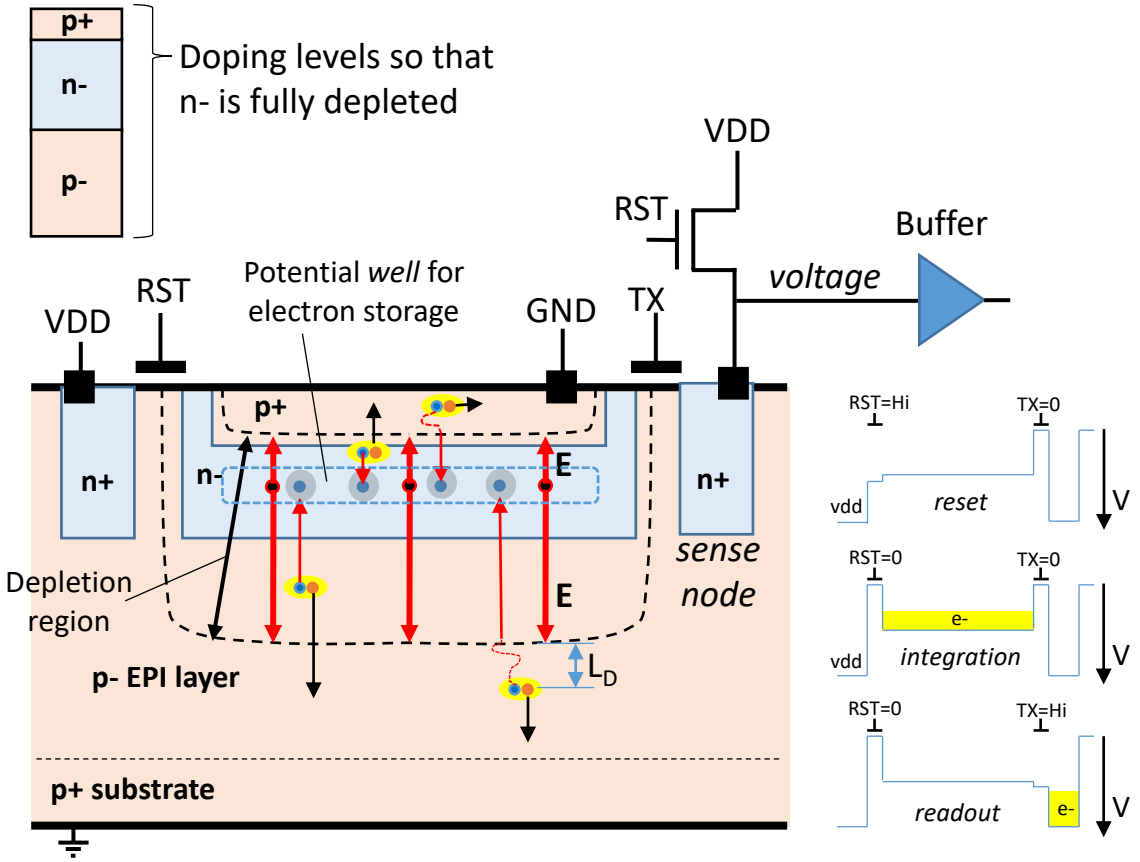
3T Photo Diode Active Pixel



Intuitive model for a pn-junction

"Collected electrons will discharge the pre-charged photo diode capacitance during the integration time. The remaining voltage over the pn-junction represents the illumination over the exposure time"

4T Pinned Photo Diode Active Pixel



Intuitive model

"Electrons are collected in a potential well during the integration time. At end of exposure the electrons are transferred to the sense node where the voltage represents the illumination over exposure time "

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